Eclipse Family Data Sheet

Combining Performance, Density, and Embedded RAM

Device Highlights

Flexible Programmable Logic

- 0.25 µ, 5 layer metal CMOS process
- 2.5 V Vcc, 2.5/3.3 V dive capable I/O
- Up to 4032 logic cells
- Up to 583,000 max system gates
- Up to 347 I/O

Embedded Dual Port SRAM

- Up to thirty-six 2,304-bit dual port SRAM blocks
- Up to 82,900 RAM bits
- RAM/ROM/FIFO Wizard for automatic configuration
- Configurable and cascadable

Applications

- Signal processing operators
- Signal processing functions
- Networking/communications for VoIP
- Speech/voice processing
- Channel coding

Programmable I/O

- High performance: <3.2 ns Tco
- Programmable slew rate control
- Programmable I/O standards:
  - LVTTL, LVCMOS, PCI, GTL+, SSTL2, and SSTL3
  - Eight independent I/O banks
  - Three register configurations: input, output and output enable

Advanced Clock Network

- Nine global clock networks
  - One dedicated
  - Eight programmable
- Sixteen I/O (high-drive) networks
- Twenty quad-net networks: five per quadrant

Figure 1: Eclipse Block Diagram

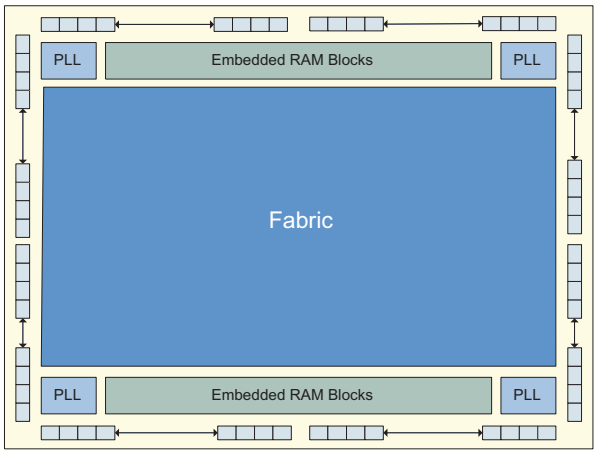


Table 1: Eclipse Product Family Members

		QL6250	QL6325	QL6500	QL6600
Max Gates		248,160	320,640	488,064	583,008
Logic Array		40x24	48x32	64x48	72x56
Logic Cells		960	1,536	3,072	4,032
Max Flip-Flops		2,670	4,002	7,185	9,105
Max I/O		250	310	347	347
RAM Modules		20	24	32	36
RAM bits		46,100	55,300	73,700	82,900
Packages	PQFP	208	208	-	-
	PBGA (1.27 mm)	-	-	516	516
	FPBGA (1.0 mm)	484	484	484	484
	LFBGA (0.8 mm)	280	280	280	280

Table 2: Max I/O per Device /Package Combination

Device	208 PQFP	280 FPBGA	484 PBGA	516 PBGA
QL6250	99	163	250	-
QL6325	99	163	310	-
QL6500	-	163	327	347
QL6600	-	163	327	347

QuickWorks Design Software

The QuickWorks® package provides the most complete ESP and FPGA software solution from design entry to logic synthesis, to place and route to simulation. The packages provide a solution for designers who use third party tools from Cadence, Mentor, OrCAD, Synopsys, Viewlogic and other third-party tools for design entry, synthesis, or simulation.

Process Data

Eclipse is fabricated on a 0.25 µm five-layer metal CMOS process. The core voltage is 2.5 V V_{CC} supply and 3.3 V tolerant I/O with the addition of 3.3 V V_{CCIO}. Eclipse is available in commercial, industrial, and military temperature grades.

Programmable Logic Architectural Overview

The Eclipse logic cell structure is presented in **Figure 2**. This architectural feature addresses current register-intensive designs.

Figure 2: Eclipse Logic Cell

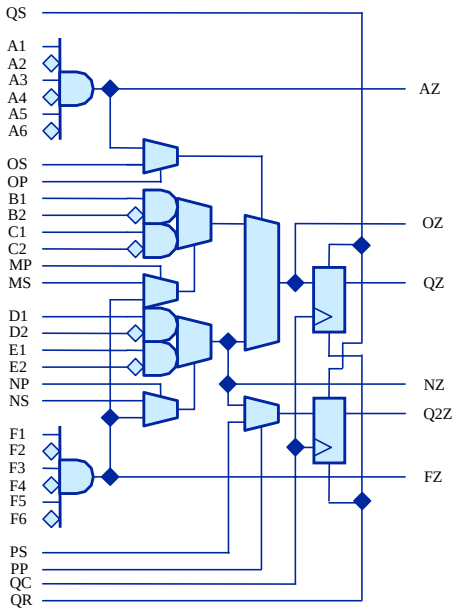


Table 3: Performance Standards

Function	Description	Slowest Speed Grade	Fastest Speed Grade
Multiplexer	16:1	5 ns	2.8 ns
Parity Tree	24	6 ns	3.4 ns
	36	6 ns	3.4 ns
Counter	16 bit	250 MHz	450 MHz
	32 bit	250 MHz	450 MHz
FIFO	128 x 32	155 MHz	280 MHz
	256 x 16	155 MHz	280 MHz
	128 x 64	155 MHz	280 MHz
Clock to Out		4.5 ns	2.5 ns
System clock		200 MHz	400 MHz

The second register has a two-to-one multiplexer controlling its input. The register can be loaded from the NZ output or directly from a dedicated input.

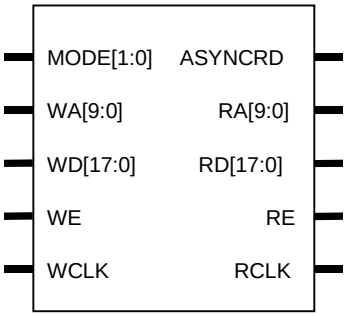
NOTE: The input “PP” is not an “input” in the classical sense. It can only be tied high or low using default links only and is used to select which path “NZ” or “PS” is used as an input to the register. All other inputs can be connected not only to “tiehi” and “tielo” but to multiple routing channels as well.

The complete logic cell consists of 2 six-input AND gates, 4 two-input AND gates, 7 two-to-one multiplexers, and 2 D flip-flop with asynchronous SET and RESET controls. The cell has a fan-in of 30 (including register control lines) and fits a wide range of functions with up to 17 simultaneous inputs. It has 6 outputs; 4 combinatorial and 2 registered. The high logic capacity and fan-in of the logic cell accommodate many user functions with a single level of logic delay while other architectures require two or more levels of delay.

RAM Modules

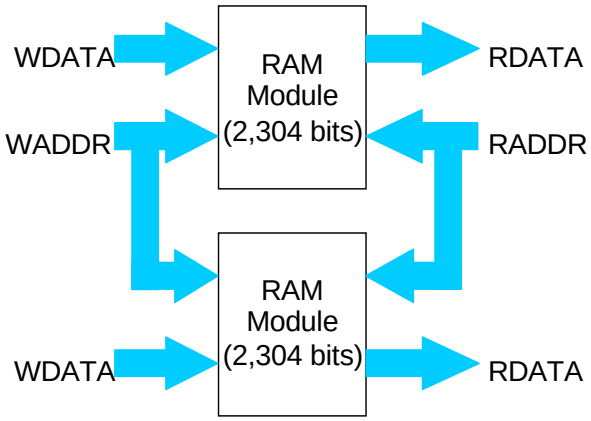
The Eclipse Family includes multiple dual-port 2,304-bit RAM modules for implementing RAM, ROM and FIFO functions. Each module is user-configurable into four different block organizations. Modules can also be cascaded horizontally to increase their effective width or vertically to increase their effective depth as shown in **Figure 3**. The RAM can also be configured as a modified Harvard Architecture, similar to those found in DSPs.

Figure 3: 2,304-bit Eclipse RAM Module



The number of RAM modules varies from 20 to 36 blocks within the Eclipse family, for a total of 46.1 to 82.9 K bits of RAM. Using two "mode" pins, designers can configure each module into 128 x 18 (Mode 0), 256 x 9 (Mode 1), 512 x 4 (Mode 2), or 1024 x 2 blocks (Mode 3). The blocks are also easily cascadable to increase their effective width and/or depth. See **Figure 4**.

Figure 4: Cascaded RAM Modules



The RAM modules are dual-port, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 10 address lines, allowing word lengths of up to 18 bits and address spaces of up to 1024 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the ninth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

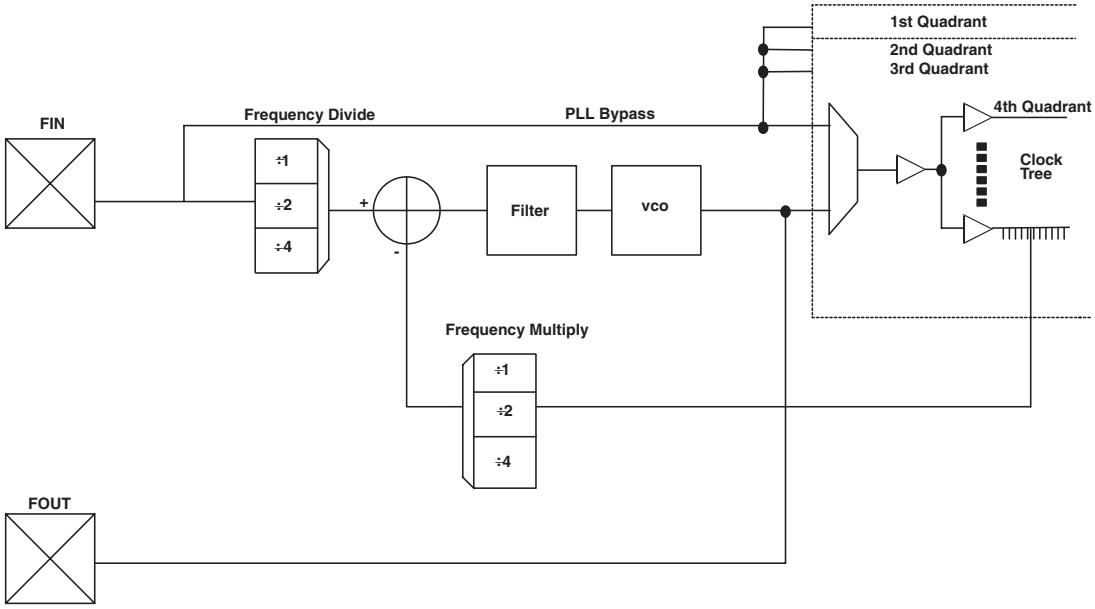
The RAM blocks can be loaded with data generated internally (typically for RAM or FIFO functions) or with data from an external PROM (typically for ROM functions).

Phase Locked Loops (PLLs)

Instead of requiring extra components, designers simply need to instantiate one of the pre-configured models described in this section and listed in **Table 4**. The QuickLogic built-in PLLs support a wider range of frequencies than many other PLLs. Also, QuickLogic PLLs can be cascaded to support different ranges of frequency multiplications or divisions, driving the device at a faster or slower rate than the incoming clock frequency. Most importantly, they achieve a very short clock-to-out time—generally less than 3 ns. This low clock-to-out time is achieved by the PLL subtracting the clock tree delay through the feedback path, effectively making the clock tree delay zero.

Figure 5 illustrates a typical QuickLogic ESP PLL.

Figure 5: PLL Block



F_{in} represents a very stable high-frequency input clock and produces an accurate signal reference. This signal can either bypass the PLL entirely, thus entering the clock tree directly, or it can pass through the PLL itself.

Within the PLL, a voltage-controlled oscillator (VCO) is added to the circuit. The external F_{in} signal and the local VCO form a control loop. The VCO is multiplied or divided down to the reference frequency, so that a phase detector (the crossed circle in **Figure 5**) can compare the two signals. If the phases of the external and local signals are not within the tolerance required, the phase detector sends a signal through the charge pump and loop filter (**Figure 5**). The charge pump generates an error voltage to bring the VCO back into alignment and the loop filter removes any high frequency noise before the error voltage enters the VCO. This new VCO signal enters the clock tree to drive the chip's circuitry.

F_{out} represents the clock signal that emerges from the output pad (the output signal PLLPAD_OUT is explained in **Table 5**). This clock signal is meaningful only when the PLL is configured for external use; otherwise, it remains in high Z state, as shown in the post-simulation waveform.

Most QuickLogic products contain four PLLs, one to be used in each quadrant. The PLL presented in **Figure 5** controls the clock tree in the fourth Quadrant of its ESP. As previously mentioned, QuickLogic PLLs compensate for the additional delay created by the clock tree itself by subtracting the clock tree delay through the feedback path.

For more specific information on the Phase Locked Loops, refer to Application Note 58 at http://www.quicklogic.com/images/appnote58.pdf.

PLL Modes of Operation

QuickLogic PLLs have eight modes of operation, based on the input frequency and desired output frequency—**Table 4** indicates the features of each mode.

Table 4: PLL Mode Frequencies

PLL Model	Output Frequency	Input Frequency Range[a]	Output Frequency Range
PLL_HF[b]	Same as input frequency	66 MHz–150 MHz	66 MHz–150 MHz
PLL_LF	Same as input frequency	25 MHz–133 MHz	25 MHz–133 MHz
PLL_MULT2HF	2 × input frequency	50 MHz–125 MHz	100 MHz–250 MHz
PLL_MULT2LF	2 × input frequency	16 MHz–50 MHz	32 MHz–100 MHz
PLL_DIV2HF	1/2 × input frequency	100 MHz–250 MHz	50 MHz–125 MHz
PLL_DIV2LF	1/2 × input frequency	50 MHz–100 MHz	25 MHz–50 MHz
PLL_MULT4	4 × input frequency	16 MHz–40 MHz	64 MHz–160 MHz
PLL_DIV4	1/4 × input frequency	100 MHz–300 MHz	25 MHz–75 MHz

a. The input frequency can range from 12.5 MHz to 500 MHz, while output frequency ranges from 25 MHz to 250 MHz. When you add PLLs to your top-level design, be sure that the PLL mode matches your desired input and output frequencies.
b. HF stands for high frequency and LF stands for low frequency.

PLL Signals

Table 5 summarizes the key signals in QuickLogic PLLs.

Table 5: PLL Signals

Signal Name	Description
PLLCLK_IN[a]	**Input clock signal**
PLLRST	**Active High Reset** If PLLRST is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work.
ONn_OFFCHIP	**PLL output** This signal selects whether the PLL will drive the internal clock network or be used off-chip. This is a static signal, not a dynamic signal. Tied to GND = outgoing signal drives internal gates. Tied to VCC = outgoing signal used off-chip.
CLKNET_OUT	**Out to internal gates** This signal bypasses the PLL logic before driving the internal gates. Note that this signal cannot be used in the same quadrant where the PLL signal is used (PLLCLK_OUT).
PLLCLK_OUT	**Out from PLL to internal gates** This signal can drive the internal gates after going through the PLL. For this to work, ONn_OFFCHIP must be tied to GND.
PLLPAD_OUT	**Out to off-chip** This outgoing signal is used off-chip. For this to work, ONn_OFFCHIP signal must be tied to VCC.
LOCK_DETECT	**Active High Lock detection signal** NOTE: For simulation purposes, this signal gets asserted after 10 clock cycles. However, it can take a maximum of 200 clock cycles to sync with the input clock upon release of the RESET signal.

a. Because PLLCLK_IN and PLLRST signals have INPAD, and PLLPAD_OUT has OUTPAD, you do not have to add additional pads to your design.

NOTE: For PLL AC specifications, contact the factory.

I/O Cell Structure

Eclipse features a variety of distinct I/O pins to maximize performance, functionality, and flexibility with bi-directional I/O pins and input-only pins. All I/O pins are 2.5 V and 3.3 V tolerant and comply with the specific I/O standard selected. All dedicated input pins are 2.5 V tolerant and comply with the LVCMOS2 standard.For single ended I/O standards, V_{CCIO} specifies the input tolerance and the output drive. For voltage referenced I/O standards (e.g., SSTL), the voltage supplied to the INREF pins in each bank specifies the input switch point. For example, the V_{CCIO} pins must be tied to a 3.3 V supply to provide 3.3 V compliance. Eclipse can also support the LVDS and LVPECL I/O standards with the use of external resistors (see **Table 6**).

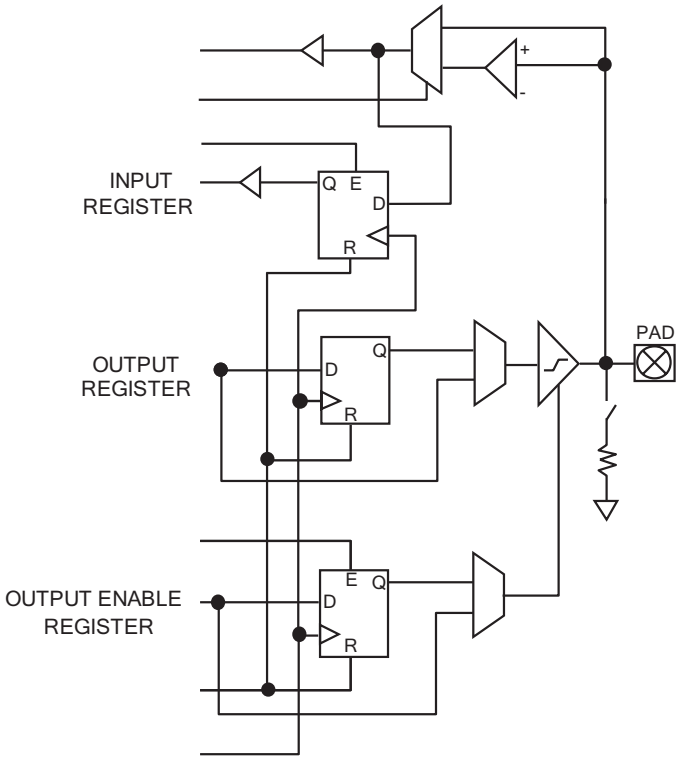
Table 6: I/O Standards and Applications

I/O Standard	INREF Reference Voltage	Output Voltage	Application
LVTTL	n/a	3.3	General Purpose
LVCMOS2	n/a	2.5	General Purpose
PCI	n/a	3.3	PCI Bus Applications
GTL+	1.0	n/a	Backplane
SSTL3	1.5	3.3	SDRAM
SSTL2	1.25	2.5	SDRAM

As designs become more complex and requirements more stringent, several application-specific I/O standards have emerged for specific applications. I/O standards for processors, memories, and a variety of bus applications have become commonplace and a requirement for many systems. In addition, I/O timing has become a greater issue with specific requirements for setup, hold, clock to out, and switching times. Eclipse has addressed these new system requirements and now includes a completely new I/O cell which consists of programmable I/Os as well as a new cell structure consisting of three registers—Input, Output, and Output Enable (OE).

Eclipse offers banks of programmable I/Os that address many of the bus standards that are popular today. As shown in **Figure 6** each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one output multiplexers.

Figure 6: Eclipse I/O Cell



The bi-directional I/O pin options can be programmed for input, output, or bi-directional operation. As shown in **Figure 6**, each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one multiplexers. The select lines of the two-to-one multiplexers are static and must be connected to either V_{CC} or GND.

For input functions, I/O pins can provide combinatorial, registered data, or both options simultaneously to the logic array. For combinatorial input operation, data is routed from I/O pins through the input buffer to the array logic. For registered input operation, I/O pins drive the D input of input cell registers, allowing data to be captured with fast set-up times without consuming internal logic cell resources. The comparator and multiplexor in the input path allows for native support of I/O standards with reference points offset from traditional ground.

For output functions, I/O pins can receive combinatorial or registered data from the logic array. For combinatorial output operation, data is routed from the logic array through a multiplexer to the I/O pin. For registered output operation, the array logic drives the D input of the output cell register which in turn drives the I/O pin through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the I/O pin. The addition of an output register will also decrease the Tco. Since the output register does not need to drive the routing the length of the output path is also reduced.

The three-state output buffer controls the flow of data from the array logic to the I/O pin and allows the I/O pin to act as an input and/or output. The buffer's output enable can be individually controlled by the logic cell array or any pin (through the regular routing resources), or it can be bank-controlled through one of the global networks. The signal can also be either combinatorial or registered. This is identical to that of the flow for the output cell. For combinatorial control operation data is routed from the logic array through a multiplexer to the three-state control. The IOCTRL pins can directly drive the OE and CLK signals for all I/O cells within the same bank.

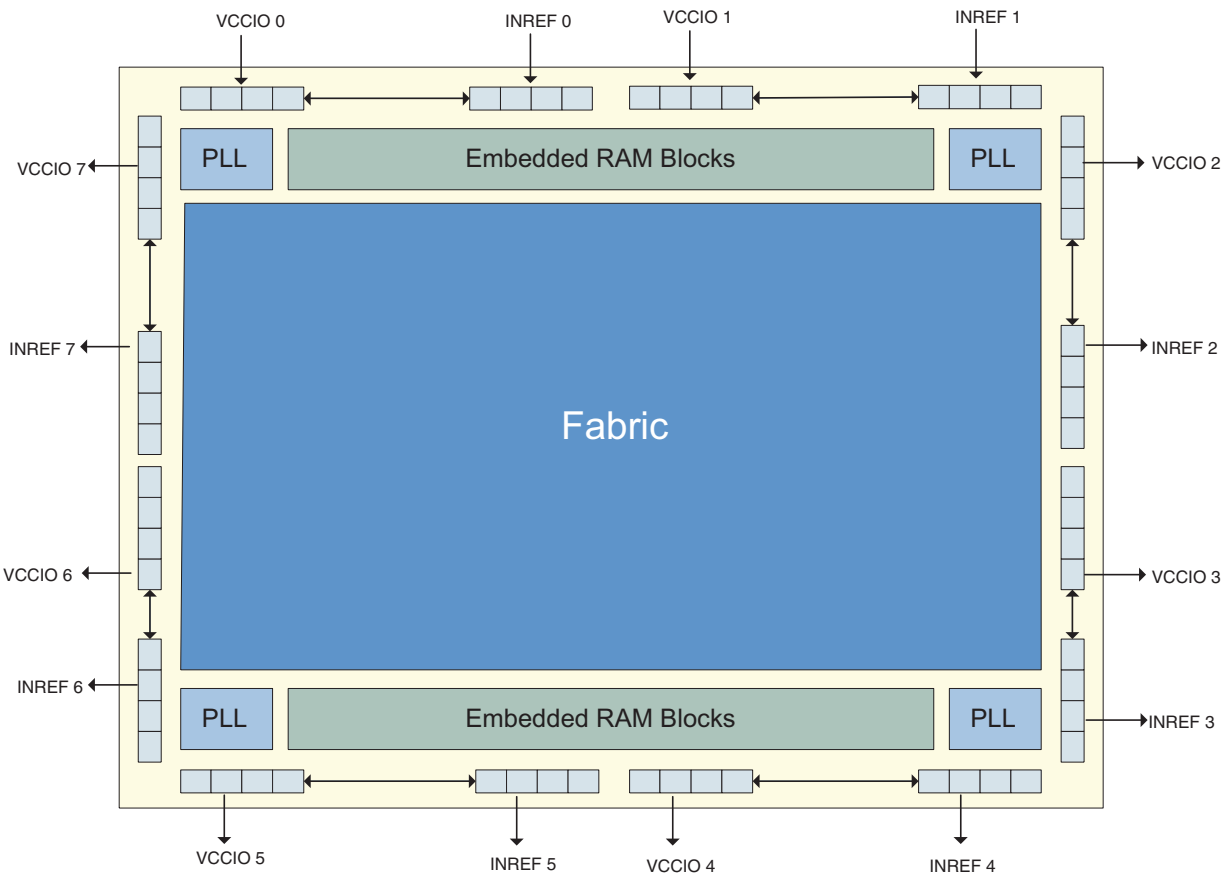
For registered control operation, the array logic drives the D input of the OE cell register which in turn drives the three-state control through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the three-state control.

When I/O pins are unused, the OE controls can be permanently disabled, allowing the output cell register to be used for registered feedback into the logic array.

I/O cell registers are controlled by clock, clock enable, and reset signals, which can come from the regular routing resources, from one of the global networks, or from two IOCTRL input pins per bank of I/Os. The CLK and RESET signals share common lines, while the clock enables for each register can be independently controlled. I/O interface support is programmable on a per bank basis. **Figure 7** illustrates the I/O bank configurations.

Each I/O bank is independent of other I/O banks and each I/O bank has its own V_{CCIO} and INREF supply inputs. A mixture of different I/O standards can be used on the device; however, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common V_{CCIO} and INREF can be shared within the same bank (e.g., PCI and LVTTL).

Figure 7: Multiple I/O Banks



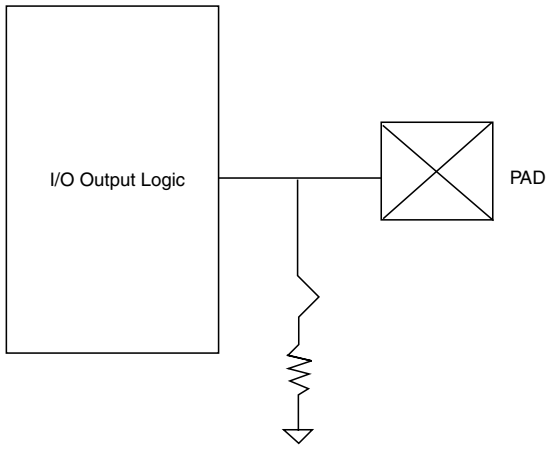
Programmable Slew Rate

Each I/O has programmable slew rate capability. The rate is programmable to one of two slew rates either fast or slow. The slower rate can be used to reduce ground bounce noise.

Programmable Weak Pull-Down

Programmable weak-pull down resistor is available on each I/O. The I/O Weak Pull-Down eliminates the need for external pull down resistor for used I/O. The spec for pull-down current is maximum of 150 µA under worst case condition.

Figure 8: Programmable I/O Weak Pull-Down

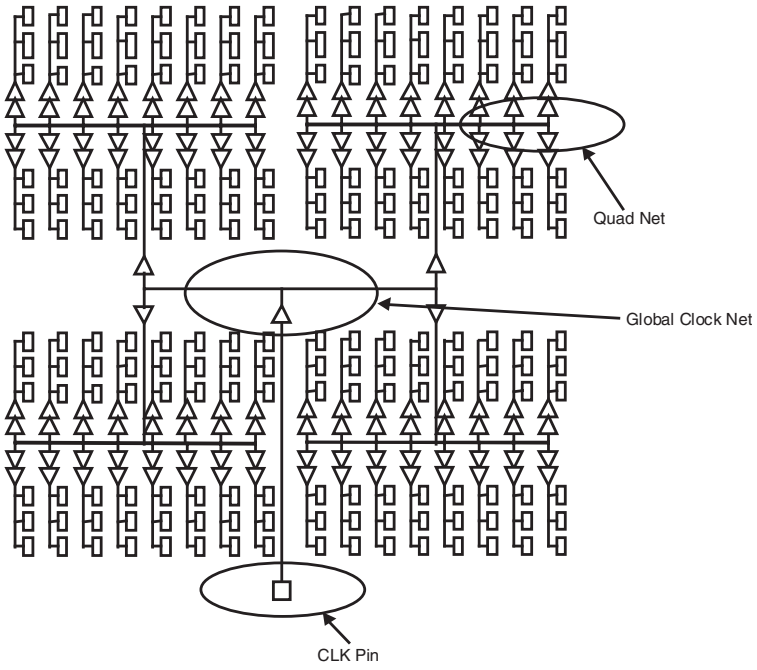


Clock Networks

Global Clocks

There are eight global clock networks in the Eclipse device family. Global clocks can drive logic cell, I/O, and RAM blocks in the device. Five global clocks have access to a Quad Net (local clock network) connection with a programmable connection to the register inputs. Global clock pins are 2.5 V, LVCMOS2, compliant.

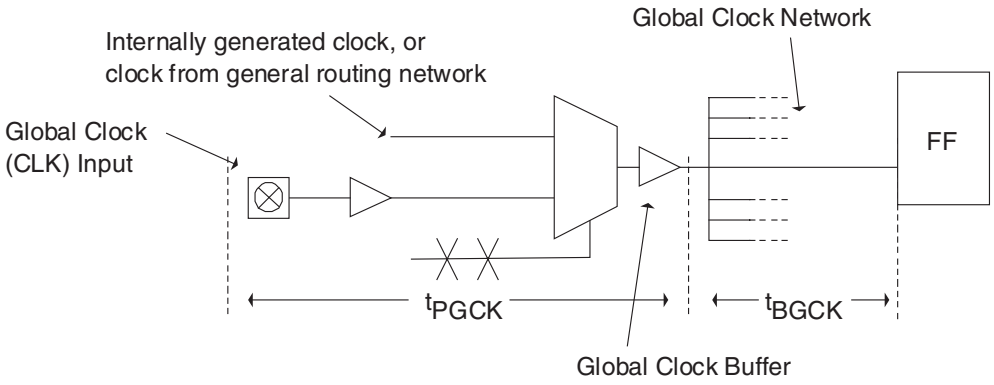
Figure 9: Global Clock Methodology



Quad-Net Network

There are five Quad-Net local clock networks in each quadrant for a total of 20 in a device. Each Quad-Net is local to a quadrant. Before driving the columns clock buffers, the quad-net is driven by the output of a mux which selects between the CLK input and an internally generated clock source (see **Figure 10**).

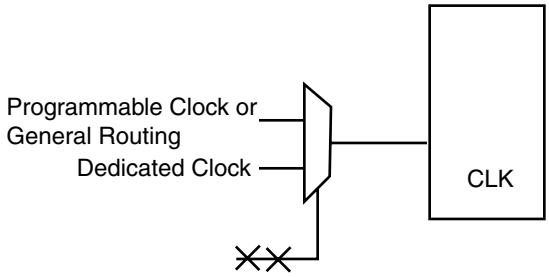
Figure 10: Global Clock Structure Schematic



Dedicated Clock

There is one dedicated clock each device of the Eclipse Family (QL6250, QL6325, QL6500, and QL6600). This clock connects to the clock input of the Logic Cell and I/O registers, and RAM blocks through a hardwired connection and is multiplexed with the programmable clock input. The dedicated clock provides a fast global network with low skew. Users have the ability to select either the dedicated clock or the programmable clock (**Figure 11**). The dedicated clock is 2.5 V, LVCMOS2, compliant.

Figure 11: Dedicated Clock Circuitry within Logic Cell



NOTE: For more information on the clocking capabilities of Eclipse FPGAs, refer to the QuickLogic Application Note 68 at http://www.quicklogic.com/images/appnote68.pdf.

I/O Control and Local Hi-Drives

Each bank of I/Os has two input-only pins that can be programmed to drive the RST, CLK and EN inputs of I/Os in that bank. These input only pins also serve as high drive inputs to a quadrant. As an I/O control or high drive, these buffers can be driven by the internal logic. I/O control pins, called IOCTRL in the pin tables, are 2.5 V, LVCMOS2, compliant.

Programmable Logic Routing

Eclipse devices are delivered with six types of routing resources as follows: short (sometimes called segmented) wires, dual wires, quad wires, express wires, distributed networks, and default wires. Short wires span the length of one logic cell, always in the vertical direction. Dual wires run horizontally and span the length of two logic cells. Short and dual wires are predominantly used for local connections. Default wires supply V_{CC} and GND (Logic '1' and Logic '0') to each column of logic cells.

Quad wires have passive link interconnect elements every fourth logic cell. As a result, these wires are typically used to implement intermediate length or medium fan-out nets.

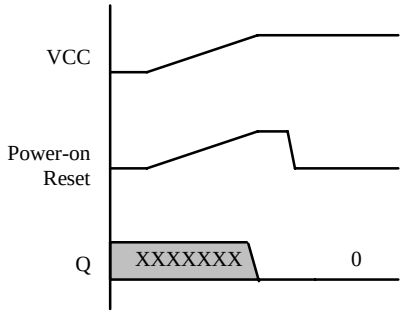
Express lines run the length of the programmable logic uninterrupted. Each of these lines has a higher capacitance than a quad, dual, or short wire, but less capacitance than shorter wires connected to run the length of the device. The resistance is lower because the express wires do not require the use of "pass" links. Express wires provide higher performance for long routes or high fan-out nets.

Distributed networks are described in the clock/control section. These wires span the programmable logic and are driven by "column clock" buffers. All clock network pin buffers (Dedicated and Global) are hard wired to individual sets of column clock buffers.

Global POR (Power-On Reset)

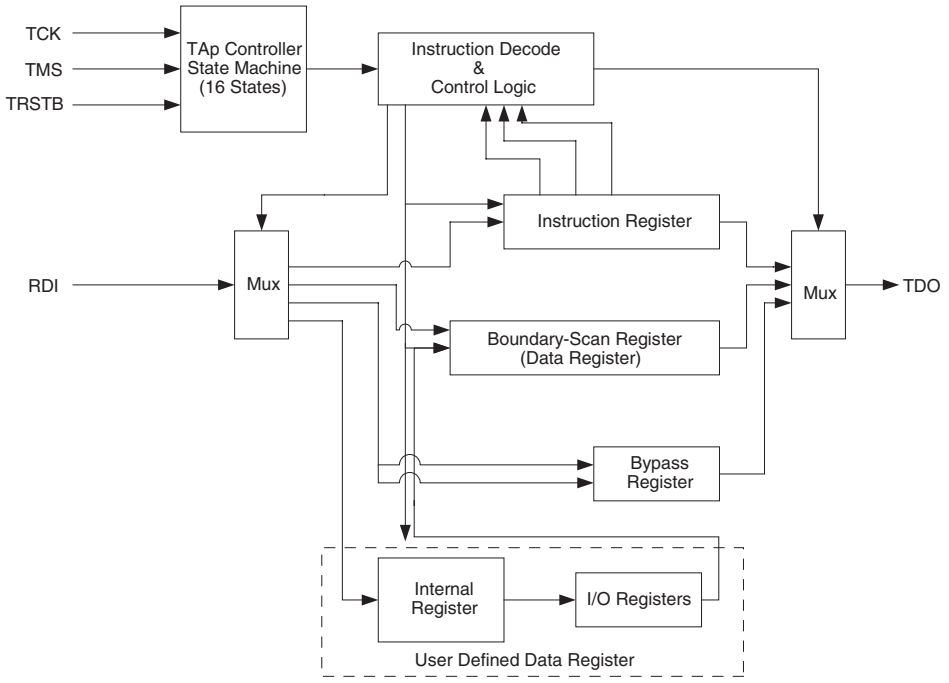
The Eclipse family of devices features a global power-on reset. This reset is hardwired to all registers and resets them to Logic '0' upon power-up of the device. In QuickLogic devices, the asynchronous Reset input to flip-flops has priority over the Set input. Therefore, the Global POR resets all flip-flops during power-up. If you want to set the flip-flops to Logic '1', you must assert the "Set" signal after the Global POR signal has been deasserted.

Figure 12: Power-On Reset



Joint Test Access Group (JTAG)

Figure 13: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not in the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** `This instruc`tion allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.

- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- BSDL-Boundary Scan Description Language
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and Automatic Test-vector Generation (ATG)

Security Fuses

There are two security links: one to disable reading logic from the array, and the second to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs. The option to program these fuses is selectable via QuickWorks in the Tools/Options/Device Programming window in SpDE.

Flexibility Fuse

The flexibility link enables Power-Up loading of the Embedded RAM blocks. If the link is programmed, the Power Up Loading state machine is activated during power-up of the device. The state machine communicates with an external EPROM via the JTAG pins to download memory contents into the on-chip RAM. If the link is not programmed, Power-Up Loading is not enabled and the JTAG pins function as they normally would. The option to program this bit is selectable via QuickWorks in the Tools/Options/Device Programming window in SpDE. For more information on Power-Up Loading refer to QuickLogic Application Note 55 at http://www.quicklogic.com/images/appnote55.pdf.

JTAG Pin Descriptions

Table 7: JTAG Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused
TRSTB/RRO	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG
TDO/RCO	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization

NOTE: All JTAG inputs are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V). All JTAG outputs are driven by the V_{CC} rail, not V_{CCIO}. Therefore, these output pins can only drive up to V_{CC} + 0.3 V. These output pins are LVCMOS2 compliant only (2.5 V).

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 8** through **Table 12**.

Table 8: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 3.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 4.6 V	ESD Pad Protection	±2000 V
INREF Voltage	2.7 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage[a]	-0.5 V to V_{CCIO} +0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Latch-up Immunity	±100 mA		

a. All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V).

Table 9: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage		2.3	2.7	2.3	2.7	2.3	2.7	V
V_{CCIO}	I/O Input Tolerance Voltage		2.3	3.6	2.3	3.6	2.3	3.6	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-4 Speed Grade	0.42	2.3	0.43	2.16	0.47	2.11	n/a
		-5 Speed Grade	0.42	1.92	0.43	1.80	0.46	1.76	n/a
		-6 Speed Grade	0.42	1.35	0.43	1.26	0.46	1.23	n/a
		-7 Speed Grade	0.42	1.27	0.43	1.19	0.46	1.16	n/a

Table 10: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_I	I or I/O Input Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	µA
C_I	Input Capacitance[a]	-	-	8	pF
I_{OS}	Output Short Circuit Current[b]	V_o = GND $V_o = V_{CC}$	-15 40	-180 210	mA mA
I_{CC}	D.C. Supply Current[c]	$V_I, V_o = V_{CCIO}$ or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}	-	0	2	mA
I_{CCIO}(DIF)	D.C. Supply Current on V_{CCIO} for Differential I/O	-	-	-	mA
I_{REF}	D.C. Supply Current on INREF	-	-10	10	µA
I_{PD}	Pad Pull-down (programmable)	V_{CCIO} = 3.6 V	-	150	µA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.
b. Only one output at a time. Duration should not exceed 30 seconds.
c. For -4/-5/-6/-7 commercial grade devices only. See **Table 11** for more details on I_{CC} characteristics.

Table 11: I_{CC} Characteristics

Characteristic	Condition	Temperature		
		Commercial	Industrial	Military
I_{CC}	V_{CC}PLL = GND	2 mA (max)	3 mA (max)	5 mA (max)
	V_{CC}PLL = V_{CC}	3.25 mA (max)	5 mA (max)	10 mA (max)

NOTE: If PLLs are not used, the V_{CC}PLL and PLLRST pins may be grounded to the lower I_{CC} for the device.

Table 12: DC Input and Output Levels

	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.0	V_{CCIO} + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	V_{CCIO} + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	V_{CCIO} + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.5	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	V_{CCIO} + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	V_{CCIO} + 0.3	1.10	1.90	8	-8

NOTE: The data provided in **Table 12** are JEDEC and PCI Specifications. QuickLogic devices either meet or exceed these requirements.

NOTE: All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V).

I/O Characteristics

Figure 14: IOL vs. VOL

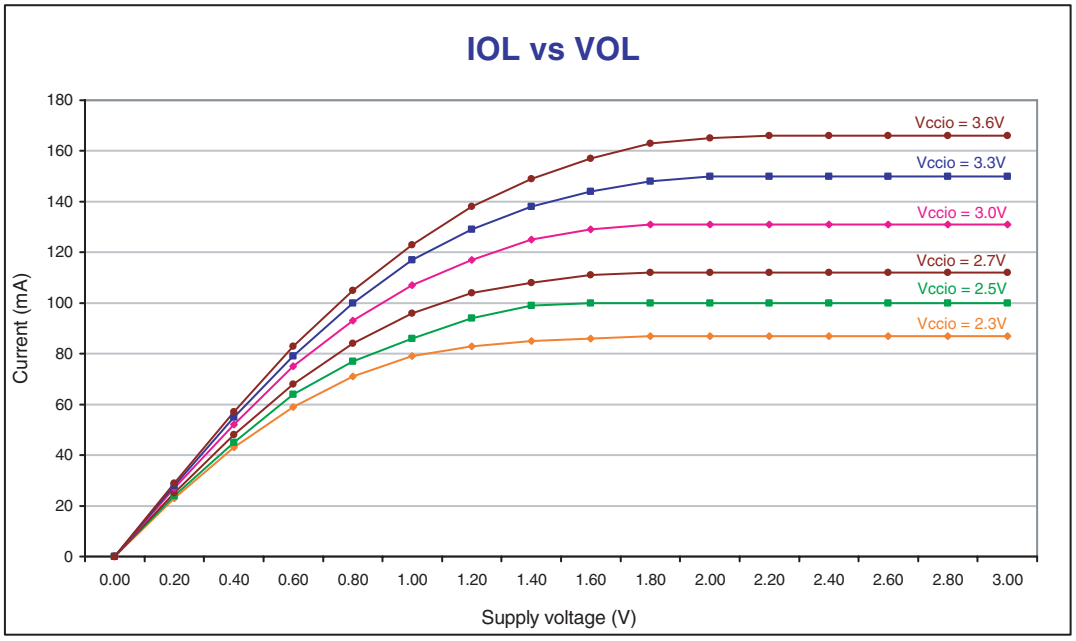
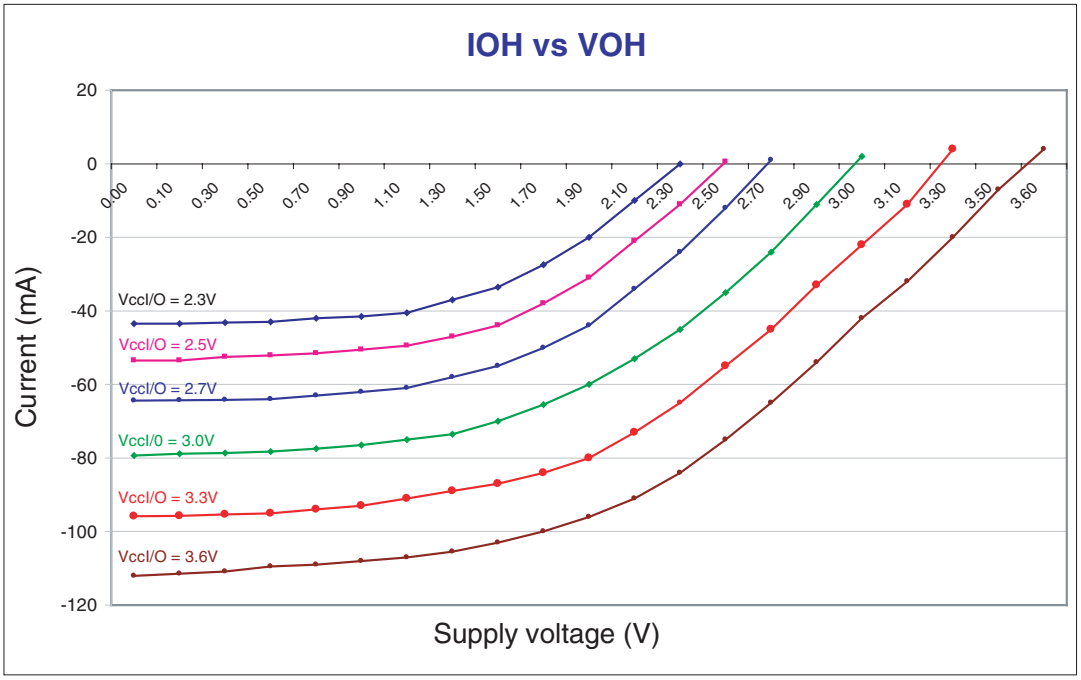


Figure 15: IOH vs. VOH



AC Characteristics at V_{CC} = 2.5 V, TA = 25° C (K = 1.00)

The AC Specifications are provided from **Table 13** to **Table 21**. Logic Cell diagrams and waveforms are provided from **Figure 16** to **Figure 21**.

Figure 16: Eclipse Logic Cell

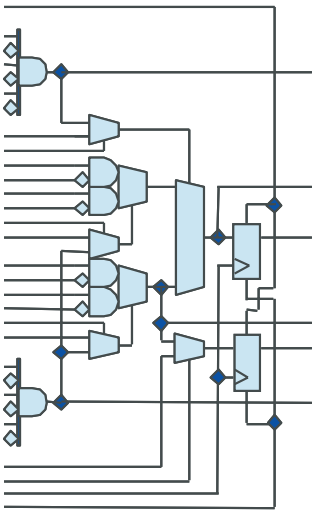


Table 13: Logic Cells

Symbol	Parameter	Value	
		Min.	Max.
t_{PD}	**Combinatorial Delay of the longest path:** time taken by the combinatorial circuit to output	0.205 ns	1.01 ns
t_{SU}	**Setup time:** time the synchronous input of the flip flop must be stable before the active clock edge	0.231 ns	-
t_{HL}	**Hold time:** time the synchronous input of the flip flop must be stable after the active clock edge	0 ns	-
t_{CO}	**Clock to out delay:** the amount of time taken by the flip flop to output after the active clock edge.	-	0.427 ns
t_{CWHI}	**Clock High Time:** required minimum time the clock stays high	0.46 ns	-
t_{CWLO}	**Clock Low Time:** required minimum time that the clock stays low	0.46 ns	-
t_{SET}	**Set Delay:** time between when the flip flop is “set” (high) and when the output is consequently “set” (high)	-	0.585 ns
t_{RESET}	**Reset Delay:** time between when the flip flop is “reset” (low) and when the output is consequently “reset” (low)	-	0.658 ns
t_{SW}	**Set Width:** time that the SET signal remains high/low	0.3 ns	-
t_{RW}	**Reset Width:** time that the RESET signal remains high/low	0.3 ns	-

Figure 17: Logic Cell Flip Flop

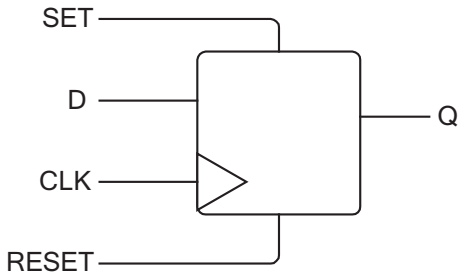


Figure 18: Logic Cell Flip Flop Timings - First Waveform

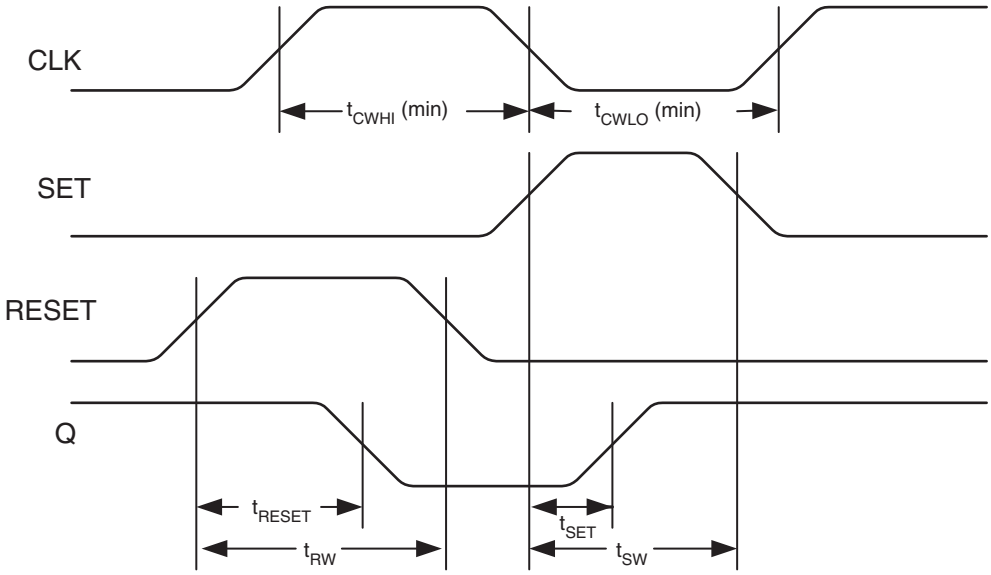


Figure 19: Logic Cell Flip Flop Timings - Second Waveform

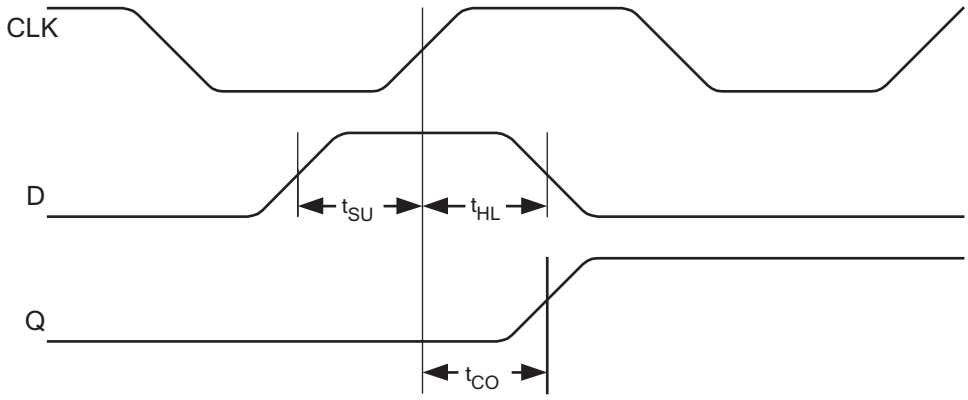


Figure 20: Eclipse Global Clock Structure

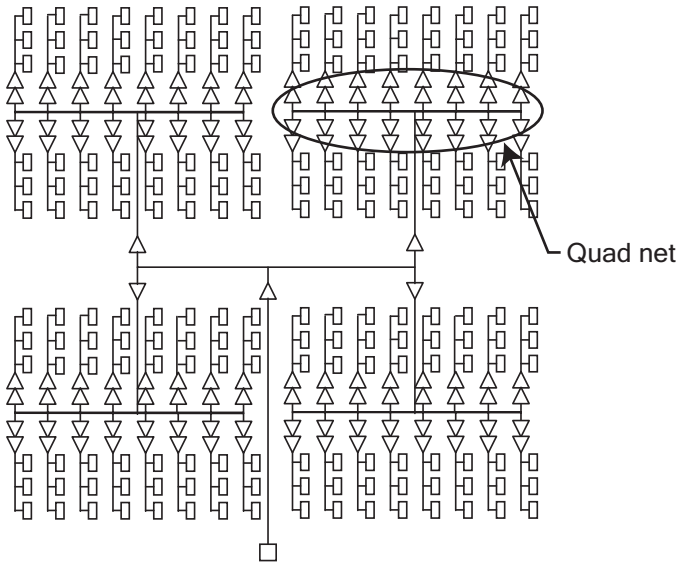


Table 14: Eclipse Global Clock Tree Delays

Clock Segment	Parameter	Value	
		Max. Rise	Max. Fall
t_{PGCK}	Global clock pin delay to quad net	0.990 ns	1.386 ns
t_{BGCK}	Global clock buffer delay (quad net to flip flop)	0.534 ns	1.865 ns

Figure 21: Global Clock Structure Schematic

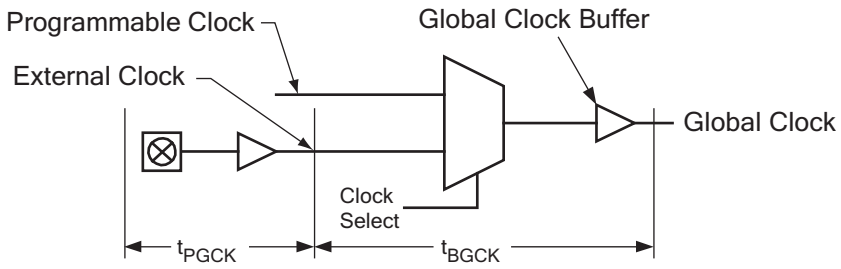


Figure 22: RAM Module

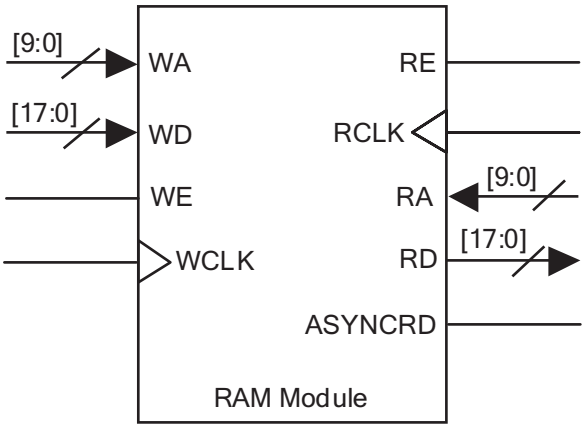


Table 15: RAM Cell Synchronous Write Timing

Symbol	Parameter	Value	
		Min.	Max.
RAM Cell Synchronous Write Timing			
t_{SWA}	**WA setup time to WCLK:** time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675 ns	-
t_{HWA}	**WA hold time to WCLK:** time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWD}	**WD setup time to WCLK:** time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654 ns	-
t_{HWD}	**WD hold time to WCLK:** time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWE}	**WE setup time to WCLK:** time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.276 ns	-
t_{HWE}	**WE hold time to WCLK:** time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{WCRD}	**WCLK to RD (WA = RA):** time between the active WRITE CLOCK edge and the time when the data is available at RD	-	2.796 ns

Figure 23: RAM Cell Synchronous Write Timing

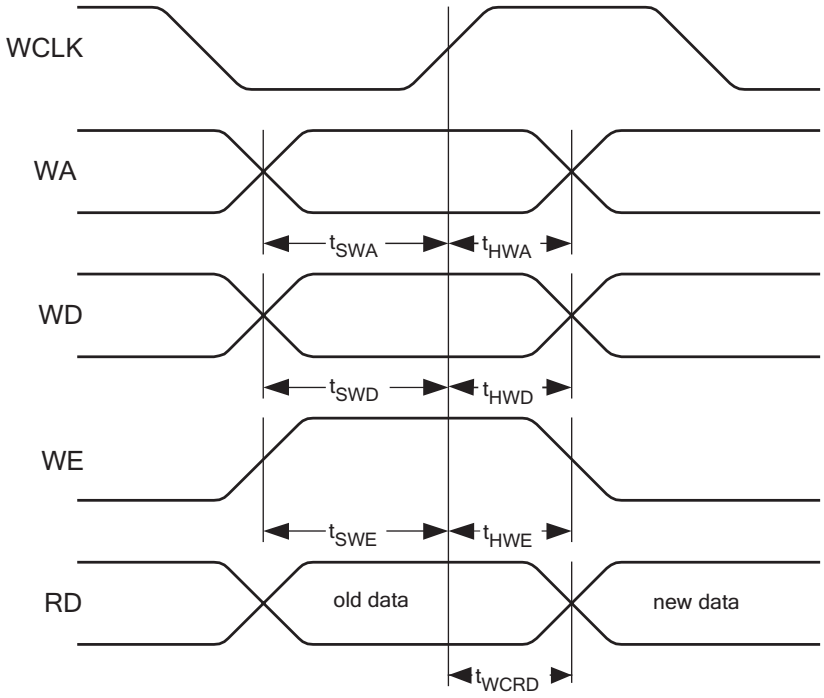


Table 16: RAM Cell Synchronous and Asynchronous Read Timing

Symbol	Parameter	Value	
		Min.	Max.
RAM Cell Synchronous Read Timing			
t_{SRA}	**RA setup time to RCLK:** time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686 ns	-
t_{HRA}	**RA hold time to RCLK:** time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	-
t_{SRE}	**RE setup time to WCLK:** time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243 ns	-
t_{HRE}	**RE hold time to WCLK:** time the READ ENABLE must be stable after the active edge of the READ CLOCK	0 ns	-
t_{RCRD}	**RCLK to RD:** time between the active READ CLOCK edge and the time when the data is available at RD	-	2.225 ns
RAM Cell Asynchronous Read Timing			
r_{PDRD}	**RA to RD:** time between when the READ ADDRESS is input and when the DATA is output	-	2.405 ns

Figure 24: RAM Cell Synchronous and Asynchronous Read Timing

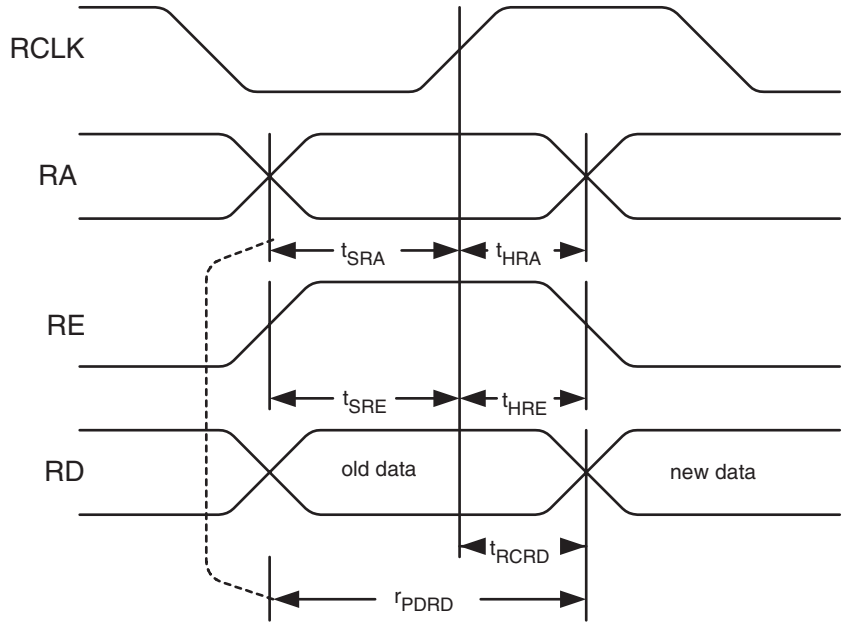


Figure 25: Eclipse Cell I/O

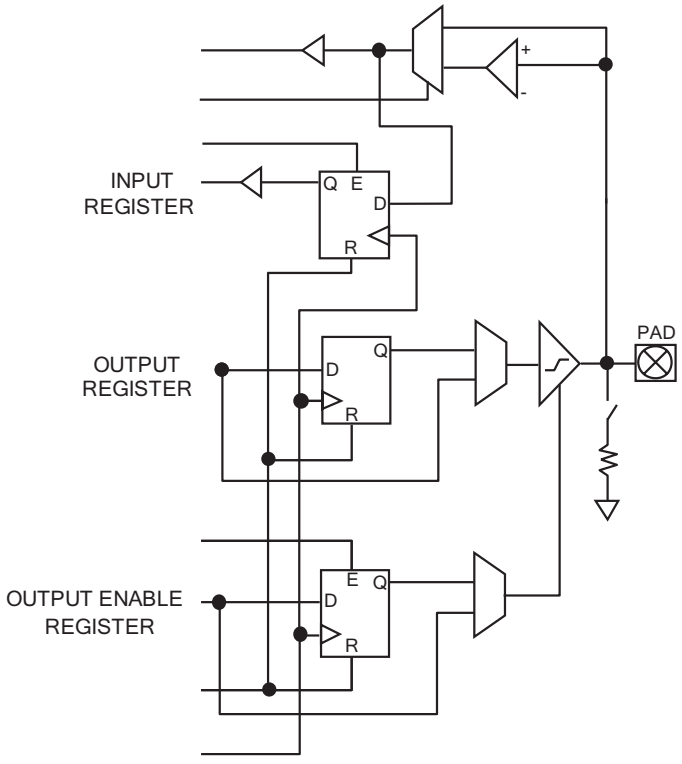


Figure 26: Eclipse Input Register Cell

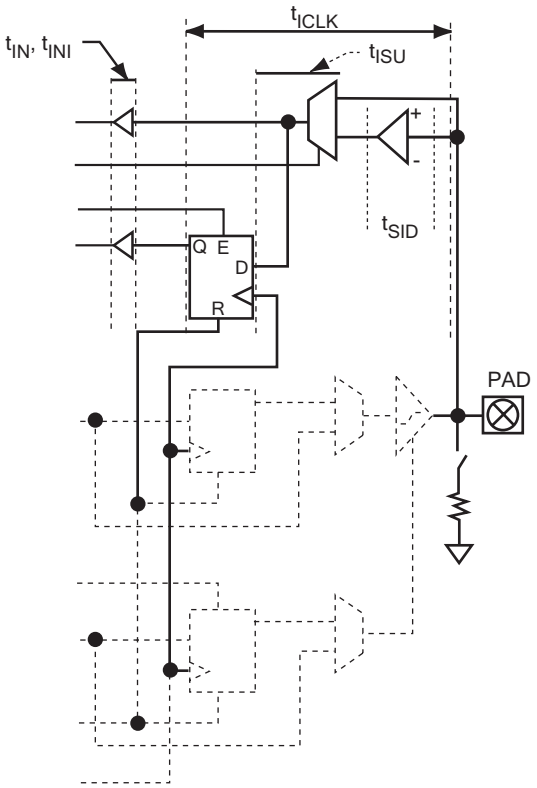


Table 17: Input Register Cell

Symbol	Parameter	Value	
		Min.	Max.
t_{ISU}	**Input register setup time:** time the synchronous input of the pin must be stable before the active clock edge	3.308 ns	3.526 ns
t_{IHL}	**Input register hold time:** time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{ICO}	**Input register clock to out:** time taken by the flip-flop to output after the active clock edge	-	0.494 ns
t_{IRST}	**Input register reset delay:** time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	-	0.464 ns
t_{IESU}	**Input register clock enable setup time:** time “enable” must be stable before the active clock edge	0.830 ns	0.987 ns
t_{IEH}	**Input register clock enable hold time:** time “enable” must be stable after the active clock edge	0 ns	-

Table 18: Standard Input Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min.	Max.
t_{SID} (LVTTL)	**LVTTL input delay:** Low Voltage TTL for 3.3 V applications	-	0.34 ns
t_{SID} (LVCMOS2)	**LVCMOS2 input delay:** Low Voltage CMOS for 2.5 V and lower applications	-	0.42 ns
t_{SID} (GTL+)	**GTL+ input delay:** Gunning Transceiver Logic	-	0.68 ns
t_{SID} (SSTL3)	**SSTL3 input delay:** Stub Series Terminated Logic for 3.3 V	-	0.55 ns
t_{SID} (SSTL2)	**SSTL2 input delay:** Stub Series Terminated Logic for 2.5 V	-	0.61 ns

Figure 27: Eclipse Input Register Cell Timing

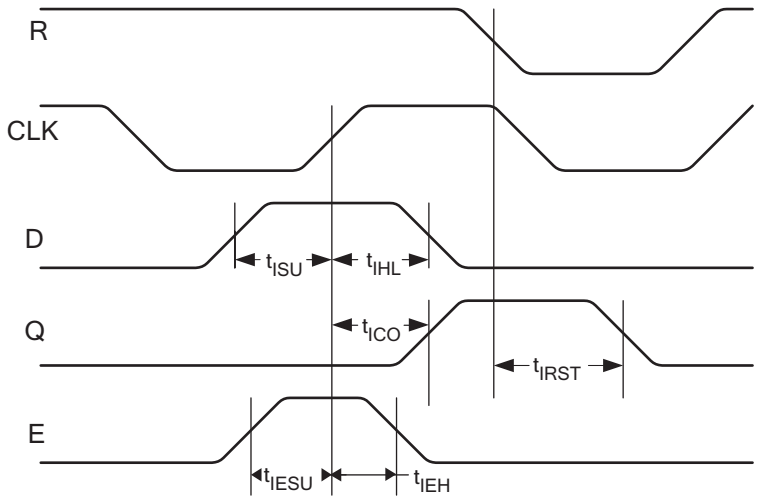


Figure 28: Eclipse Output Register Cell

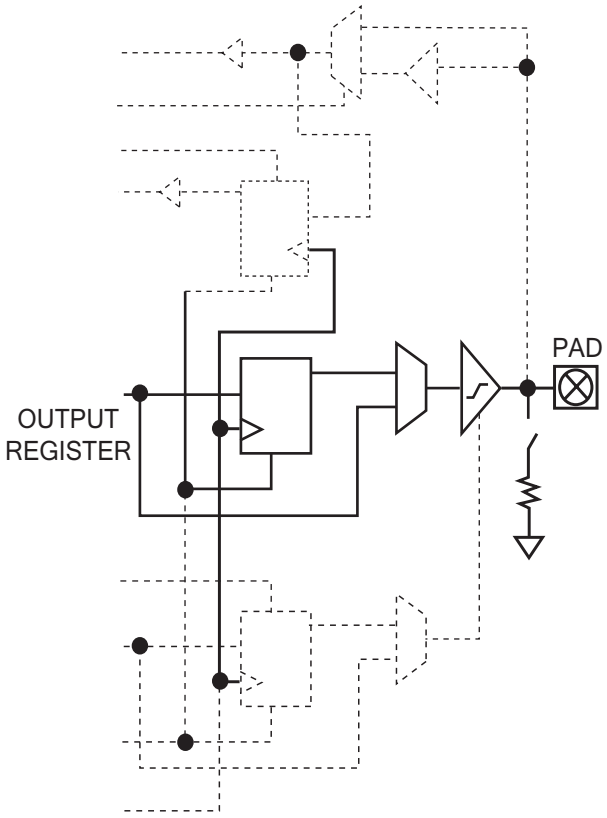


Table 19: Eclipse Output Register Cell

Symbol	Parameter	Value	
Output Register Cell Only		**Min.**	**Max.**
t_{OUTLH}	Output Delay low to high (90% of H)	-	2.594 ns
t_{OUTHL}	Output Delay high to low (10% of L)	-	2.163 ns
t_{PZH}	Output Delay tri-state to high (90% of H)	-	3.056 ns
t_{PZL}	Output Delay tri-state to low (10% of L)	-	2.709 ns
t_{PHZ}	Output Delay high to tri-State	-	3.434 ns
t_{PLZ}	Output Delay low to tri-State	-	3.318 ns
t_{COP}	Clock to out delay (does not include clock tree delays)	-	2.667 ns (fast slew) 8.999 ns (slow slew)

Figure 29: Eclipse Output Register Cell Timing

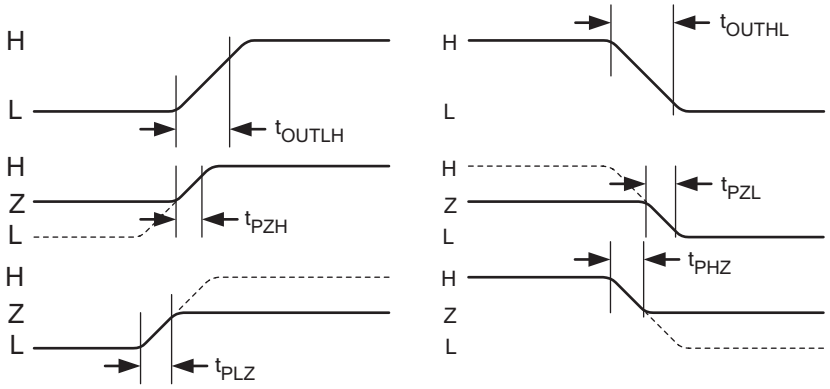


Table 20: Output Slew Rates @ V_{CCIO} = 3.3 V

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 21: Output Slew Rates @ V_{CCIO} = 2.5 V

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

NOTE: For tips to minimize ground bounce, refer to Application Note 66 at http://www.quicklogic.com/images/appnote66.pdf.

Package Thermal Characteristics

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$

$\theta_{JA} = (TJ - TA)/P$

$P_{MAX} = (T_{JMAX} - T_{AMAX})/ \theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 150°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 22**, pick an appropriate T_{AMAX} and use:

$P_{MAX} = (150°C - T_{AMAX})/ \theta_{JA}$

Table 22: Package Thermal Characteristics

Package Description		θ_{JA} (º C/W) @ various flow rates (m/sec)				θ_{JC} (º C/W)
Pin Count	Package Type	0	0.5	1	2	
516	PBGA	20.0	19.0	17.5	16.0	7.0
484	PBGA	28.0	26.0	25.0	23.0	9.0
280	LFBGA	18.5	17.0	15.5	14.0	7.0
208	PQFP	26.0	24.5	23.0	22.0	11.0

Kv and Kt Graphs

Figure 30: Voltage Factor vs. Supply Voltage

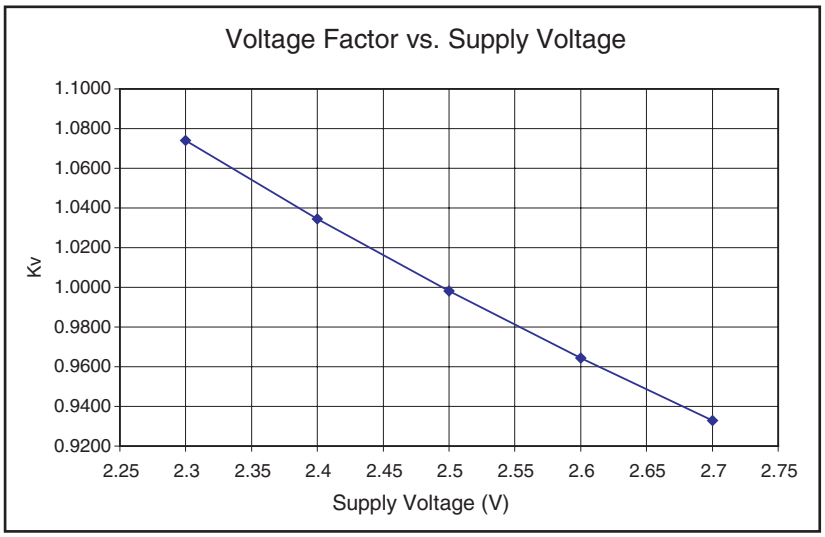
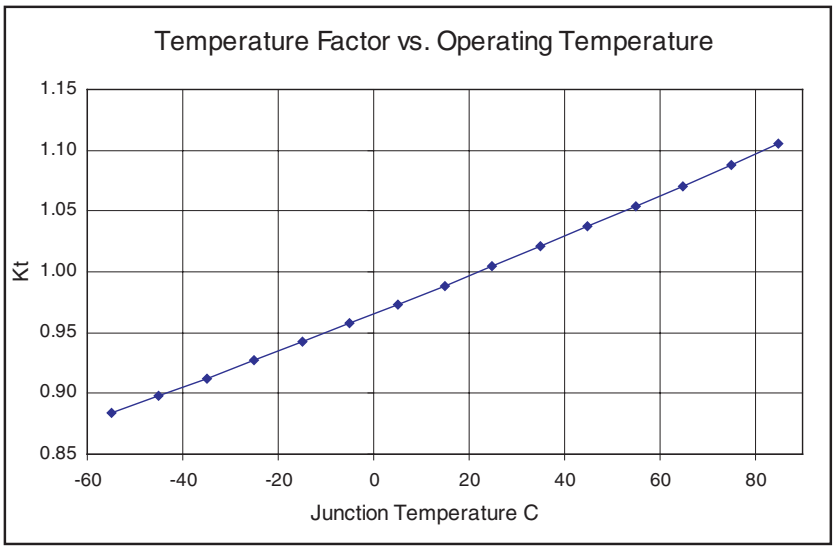


Figure 31: Temperature Factor vs. Operating Temperature



Power vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{TOTAL} = 0.350 + f[0.0031\ \eta_{LC} + 0.0948\ \eta_{CKBF} + 0.01\ \eta_{CLBF} + 0.0263\ \eta_{CKLD} + 0.543\ \eta_{RAM} + 0.20\ \eta_{PLL} + 0.0035\ \eta_{INP} + 0.0257\ \eta_{OUTP}]\ (mW)$$

Where:

η_{LC} is the total number of logic cells in the design

η_{CKBF} = # of clock buffers

η_{CLBF} = # of column clock buffers

η_{CKLD} = # of loads connected to the column clock buffers

η_{RAM} = # of RAM blocks

η_{PLL} = # of PLLs

η_{INP} is the number of input pins

η_{OUTP} is the number of output pins

Figure 32 exhibits the power consumption in an Eclipse device. The chip was filled with (300) 8-bit counters (approximately 76% logic cell utilization).

Figure 32: Power Consumption

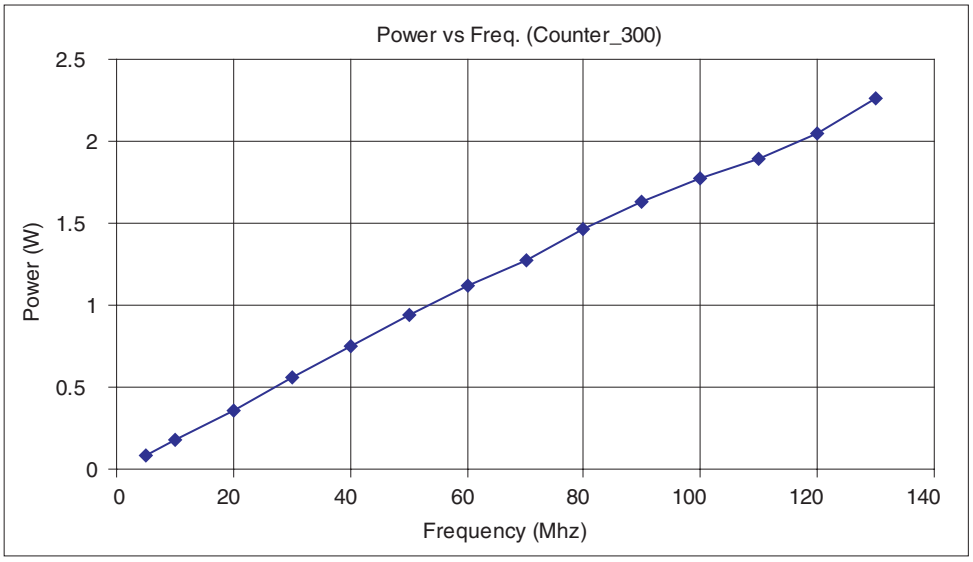
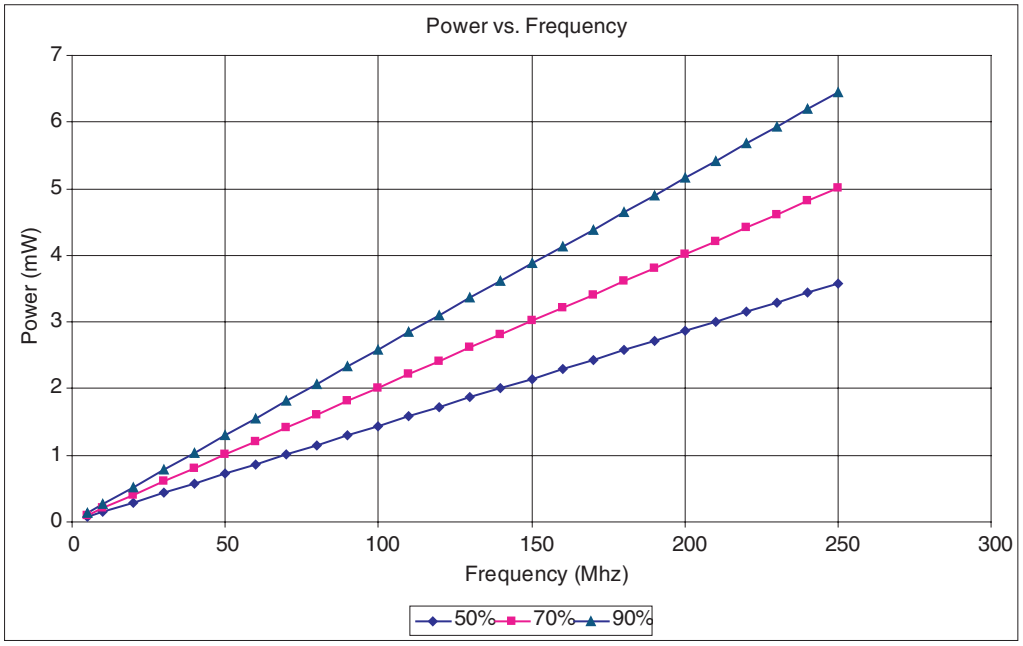


Figure 33 illustrates the theoretical worst-case scenarios for 50%, 70%, and 90% utilizations of the QL6600-516 package. The resources of the device are divided exactly in half; meaning, for 50% utilization, exactly 50% of the I/Os, Logic Cells, RAM blocks, clock network, etc. are utilized. These situations may never occur in a real design, but they do provide a very rough quantitative measure of power consumption when talking in terms of 50% or 70% utilization of an Eclipse device.

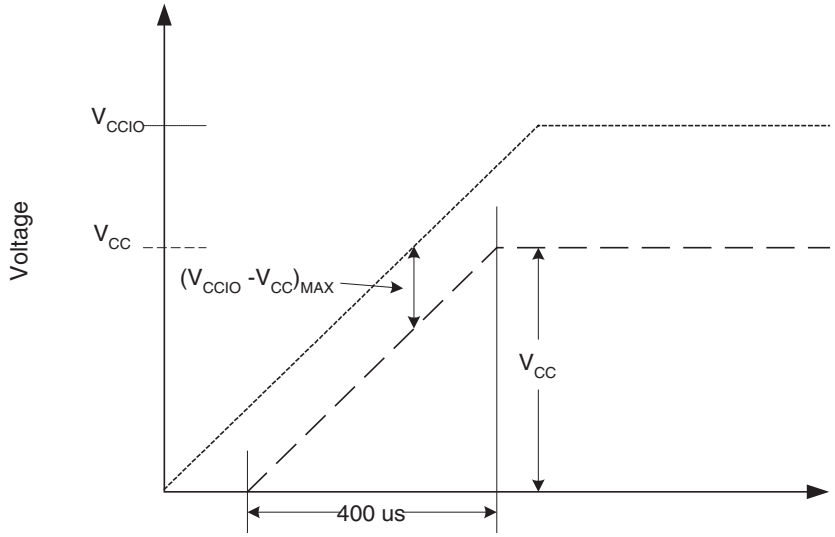
Figure 33: Power vs. Frequency (Absolute 50%, 70%, and 90% of the Available Resources on Chip)



To learn more about power consumption, refer to Application Note 60 which is located at http://www.quicklogic.com/images/appnote60.pdf.

Power-Up Sequencing

Figure 34: Power-Up Requirements/Recommendations



When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 µs or longer to reach the maximum value (refer to **Figure 34**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

Pin Descriptions

Table 23 describes the pins/balls of all Eclipse devices.

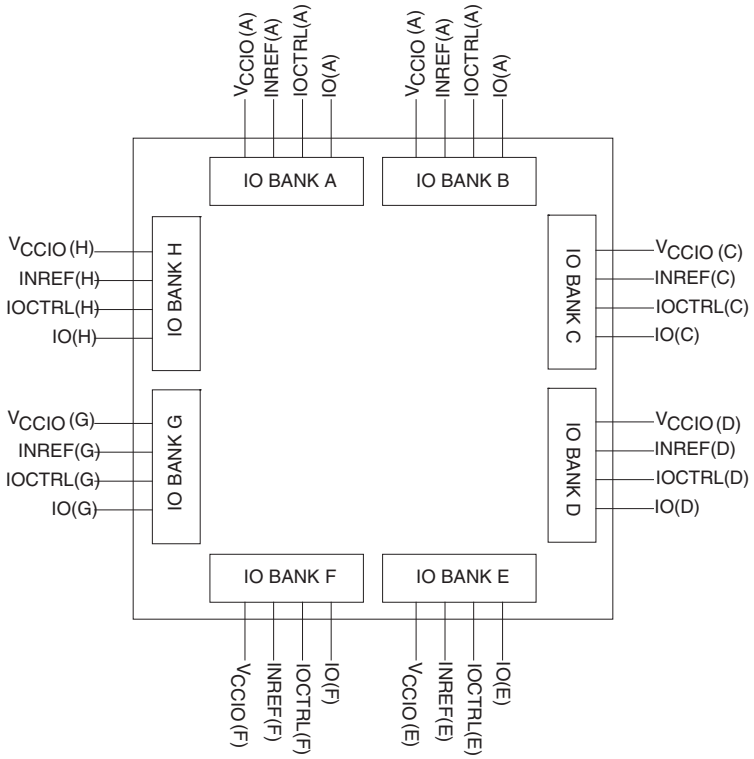
Table 23: Dedicated Pin Descriptions

Pin	Direction	Function	Description
CLK[a]	I	Global clock network driver	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and Output Enables of the I/Os.
I/O(A)	I/O	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (Quick*Works* Tool) provides the option of tying that pin to GND, $V_{CC,}$ or TriState during programming.
V_{CC}	I	Power supply pin	Connect to 2.5 V supply.
V_{CCIO}(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V device or a 2.5 V device. The A inside the parenthesis means that V_{CCIO} is located in BANK A. Every I/O pin in Bank A will be tolerant of V_{CCIO} input signals and will output V_{CCIO} level signals. This pin must be connected to either 3.3 V or V_{CC}.
V_{CC}PLL[b]	I	Phase locked loop power supply pin	Connect to 2.5 V supply. VCCPLL should be connected to 2.5 V supply if the PLLs are used. If the PLLs are not used, V_{CC}PLL can be connected to 2.5 V supply or GND. See **Table 11** for I_{CC} differences when V_{CC}PLL is connected to 2.5 V or GND.
GND	I	Ground pin	Connect to ground.
PLLIN[a]	I	PLL clock input	Clock input for PLL.
DEDCLK[a]	I	Dedicated clock pin	Low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of all sequential elements of the device (e.g., RAM and flip-flops).
GNDPLL	I	Ground pin for PLL	Connect to GND.
INREF(A)	I	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in **Table 18** for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if not needed.
PLLOUT[b]	O	PLL output pin	Dedicated PLL output pin. Otherwise may be left unconnected.
PLLRST[a]	I	Reset input pin for PLL	Reset input for PLL. If PLLs are not used, PLLRST should be connected to the same voltage as V_{CC}PLL (e.g., V_{CC} or GND).
IOCTRL(A)[a]	I	Highdrive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. This pin should be tied to GND or V_{CC} if it is not used.

a. All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V).

b. All PLLOUT output pins are driven by the V_{CC} rail, not the V_{CCIO} rail. These output pins are LVCMOS2 compliant only (2.5 V).

Figure 35: I/O Banks with Relevant Pins



Recommended Unused Pin Terminations for the Eclipse Devices

All unused, general purpose I/O pins can be tied to V_{CC}, GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint→Fix Placement** in the Option pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 24**.

Table 24: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x>	For low power unused PLL output pins can be connected to V_{CC} or GND so that their associated input buffer never floats, otherwise PLL output pins can be left unconnected. Utilized PLL output pins that route the PLL clock outside of the chip should not be tied to either V_{CC} or GND.
IOCTRL<y>	Any unused pins of this type must be connected to either V_{CC} or GND.
CLK/PLLIN<x>	Any unused clock pins should be connected to V_{CC} or GND.
PLLRST<x>	If a PLL module is not used, then the associated PLLRST<x> must be connected to V_{CC}; under normal operation, use it as needed. If PLLs are not used, the associated PLLRST pin must be connected to the same voltage as V_{CC}PLL (2.5 V or GND).
INREF<y>	If an I/O bank does not require the use of INREF signal the pin should be connected to GND.

NOTE: x -> number, y -> alphabetical character.

QL6250 - 208 PQFP Pinout Diagram

QL6250 - 208 PQFP Pinout Table

Table 25: 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	PLLRST(3)	43	IO(B)	85	IO(D)	127	CLK(5)/PLLIN(3)	169	IOCTRL(G)
2	VCCPLL(3)	44	VCCIO(B)	86	VCC	128	CLK(6)	170	INREF(G)
3	GND	45	IO(B)	87	IO(D)	129	VCC	171	IOCTRL(G)
4	GND	46	VCC	88	IO(D)	130	CLK(7)	172	IO(G)
5	IO(A)	47	IO(B)	89	VCC	131	VCC	173	IO(G)
6	IO(A)	48	IO(B)	90	IO(D)	132	CLK(8)	174	IO(G)
7	IO(A)	49	GND	91	IO(D)	133	TMS	175	VCC
8	VCCIO(A)	50	TDO	92	IOCTRL(D)	134	IO(F)	176	IO(G)
9	IO(A)	51	PLLOUT(1)	93	INREF(D)	135	IO(F)	177	VCCIO(G)
10	IO(A)	52	GNDPLL(2)	94	IOCTRL(D)	136	IO(F)	178	GND
11	IOCTRL(A)	53	GND	95	IO(D)	137	GND	179	IO(G)
12	VCC	54	VCCPLL(2)	96	IO(D)	138	VCCIO(F)	180	IO(G)
13	INREF(A)	55	PLLRST(2)	97	IO(D)	139	IO(F)	181	IO(G)
14	IOCTRL(A)	56	VCC	98	VCCIO(D)	140	IO(F)	182	VCC
15	IO(A)	57	IO(C)	99	IO(D)	141	IO(F)	183	TCK
16	IO(A)	58	GND	100	IO(D)	142	IO(F)	184	VCC
17	IO(A)	59	IO(C)	101	GND	143	IO(F)	185	IO(H)
18	IO(A)	60	VCCIO(C)	102	PLLOUT(0)	144	IOCTRL(F)	186	IO(H)
19	VCCIO(A)	61	IO(C)	103	GND	145	INREF(F)	187	IO(H)
20	IO(A)	62	IO(C)	104	GNDPLL(1)	146	VCC	188	GND
21	GND	63	IO(C)	105	PLLRST(1)	147	IOCTRL(F)	189	VCCIO(H)
22	IO(A)	64	IO(C)	106	VCCPLL(1)	148	IO(F)	190	IO(H)
23	TDI	65	IO(C)	107	IO(E)	149	IO(F)	191	IO(H)
24	CLK(0)	66	IO(C)	108	GND	150	VCCIO(F)	192	IOCTRL(H)
25	CLK(1)	67	IOCTRL(C)	109	IO(E)	151	IO(F)	193	IO(H)
26	VCC	68	INREF(C)	110	IO(E)	152	IO(F)	194	INREF(H)
27	CLK(2)/PLLIN(2)	69	IOCTRL(C)	111	VCCIO(E)	153	GND	195	VCC
28	CLK(3)/PLLIN(1)	70	IO(C)	112	IO(E)	154	IO(F)	196	IOCTRL(H)
29	VCC	71	IO(C)	113	VCC	155	PLLOUT(3)	197	IO(H)
30	CLK(4)/ DEDCLK/PLLIN(0)	72	VCCIO(C)	114	IO(E)	156	GNDPLL(0)	198	IO(H)
31	IO(B)	73	IO(C)	115	IO(E)	157	GND	199	IO(H)
32	IO(B)	74	IO(C)	116	IO(E)	158	VCCPLL(0)	200	IO(H)
33	GND	75	GND	117	IOCTRL(E)	159	PLLRST(0)	201	IO(H)
34	VCCIO(B)	76	VCC	118	INREF(E)	160	GND	202	IO(H)
35	IO(B)	77	IO(C)	119	IOCTRL(E)	161	IO(G)	203	VCCIO(H)
36	IO(B)	78	TRSTB	120	IO(E)	162	VCCIO(G)	204	GND
37	IO(B)	79	VCC	121	IO(E)	163	IO(G)	205	IO(H)
38	IO(B)	80	IO(D)	122	VCCIO(E)	164	IO(G)	206	PLLOUT(2)
39	IOCTRL(B)	81	IO(D)	123	GND	165	VCC	207	GND
40	INREF(B)	82	IO(D)	124	IO(E)	166	IO(G)	208	GNDPLL(3)
41	IOCTRL(B)	83	GND	125	IO(E)	167	IO(G)		
42	IO(B)	84	VCCIO(D)	126	IO(E)	168	IO(G)		

QL6250 - 280 LFBGA Pinout Diagram

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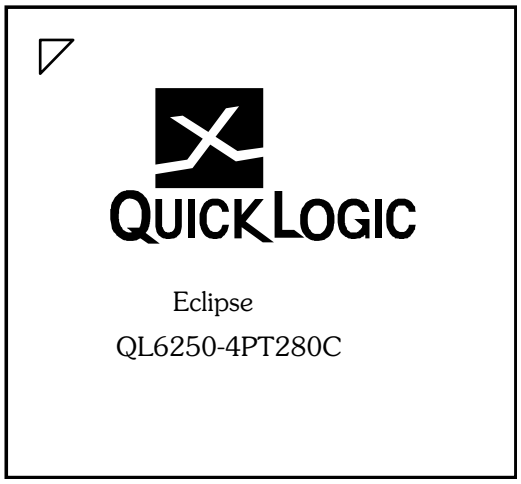

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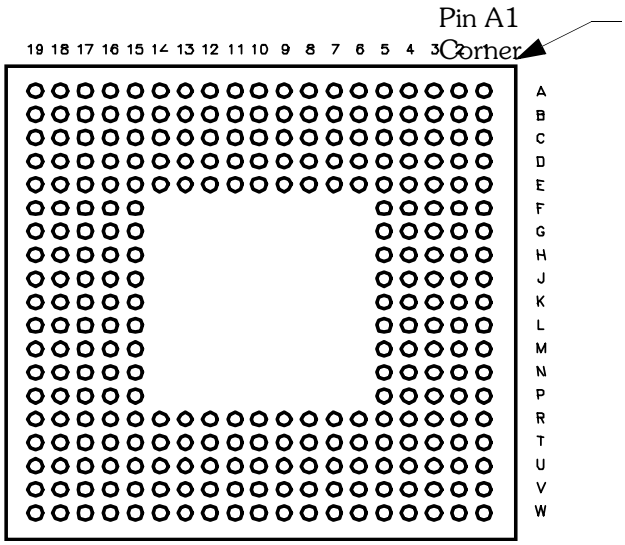

QL6250 - 280 LFBGA Pinout Table

Table 26: 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VCC	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VCC	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VCC	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

QL6250 - 484 PBGA Pinout Diagram

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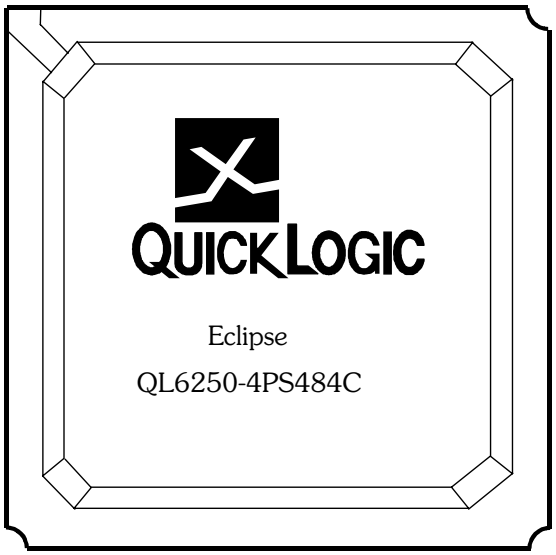

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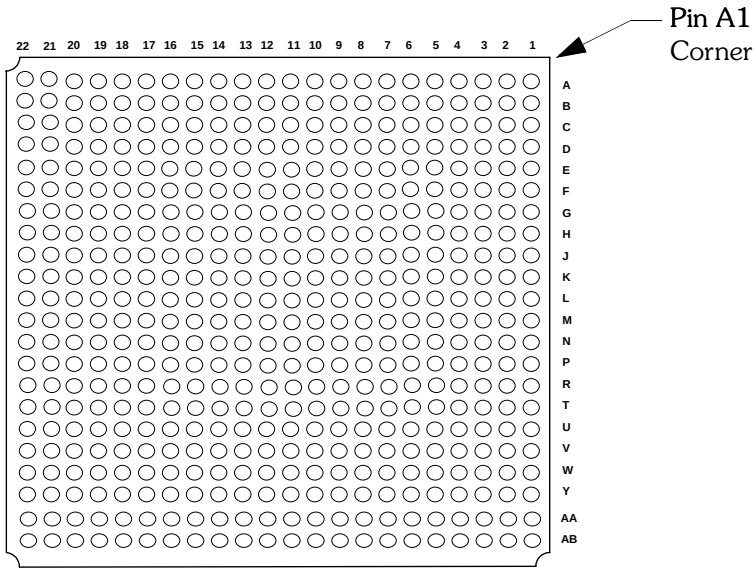

QL6250 - 484 PBGA Pinout Table

Table 27: 484 PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	NC	C1	NC	E1	IOCTRL(A)	G1	NC	J1	I/O(A)	L1	CLK(4)/ DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	NC	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	NC	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	NC	C6	NC	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	NC	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	NC	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	NC	C10	NC	E10	I/O(H)	G10	NC	J10	VCC	L10	GND
A11	NC	C11	I/O(H)	E11	VDED2	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	NC	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	NC	J13	VCC	L13	GND
A14	I/O(G)	C14	NC	E14	NC	G14	NC	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	NC	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	NC	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	NC	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	NC	G21	INREF(F)	J21	I/O(F)	L21	NC
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	NC	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	NC
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	NC	F7	VCCIO(H)	H7	I/O(H)	K7	NC	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	NC	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	NC	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	NC	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	NC	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	NC	D15	IOCTRL(G)	F15	NC	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	NC	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	NC	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	NC	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	NC	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	NC	K22	NC	M22	TMS

Table 27: 484 PBGA Pinout Table *(Continued)*

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	NC	P16	I/O(E)	T9	NC	V2	I/O(B)	W17	NC	AA10	I/O(C)
N2	I/O(B)	P17	NC	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	NC	AA12	I/O(D)
N4	NC	P19	NC	T12	NC	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	NC	W21	NC	AA14	I/O(D)
N6	NC	P21	I/O(E)	T14	NC	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	NC	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	NC
N8	VCC	R1	I/O(B)	T16	GND	V9	NC	Y2	I/O(B)	AA17	NC
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	NC	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	NC	V12	VDED2	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	NC	V13	NC	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	NC	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLRST(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	NC	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	NC	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	NC	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	NC	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	NC
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLLRST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	NC
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	NC	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	NC	W8	NC	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	NC	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	NC	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	NC	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	NC	W14	NC	AA7	NC	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	NC	AA9	NC		

QL6325 - 208 PQFP Pinout Diagram

QL6325 - 208 PQFP Pinout Table

Table 28: 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	PLLRST(3)	43	IO(B)	85	IO(D)	127	CLK(5)/PLLIN(3)	169	IOCTRL(G)
2	VCCPLL(3)	44	VCCIO(B)	86	VCC	128	CLK(6)	170	INREF(G)
3	GND	45	IO(B)	87	IO(D)	129	VCC	171	IOCTRL(G)
4	GND	46	VCC	88	IO(D)	130	CLK(7)	172	IO(G)
5	IO(A)	47	IO(B)	89	VCC	131	VCC	173	IO(G)
6	IO(A)	48	IO(B)	90	IO(D)	132	CLK(8)	174	IO(G)
7	IO(A)	49	GND	91	IO(D)	133	TMS	175	VCC
8	VCCIO(A)	50	TDO	92	IOCTRL(D)	134	IO(F)	176	IO(G)
9	IO(A)	51	PLLOUT(1)	93	INREF(D)	135	IO(F)	177	VCCIO(G)
10	IO(A)	52	GNDPLL(2)	94	IOCTRL(D)	136	IO(F)	178	GND
11	IOCTRL(A)	53	GND	95	IO(D)	137	GND	179	IO(G)
12	VCC	54	VCCPLL(2)	96	IO(D)	138	VCCIO(F)	180	IO(G)
13	INREF(A)	55	PLLRST(2)	97	IO(D)	139	IO(F)	181	IO(G)
14	IOCTRL(A)	56	VCC	98	VCCIO(D)	140	IO(F)	182	VCC
15	IO(A)	57	IO(C)	99	IO(D)	141	IO(F)	183	TCK
16	IO(A)	58	GND	100	IO(D)	142	IO(F)	184	VCC
17	IO(A)	59	IO(C)	101	GND	143	IO(F)	185	IO(H)
18	IO(A)	60	VCCIO(C)	102	PLLOUT(0)	144	IOCTRL(F)	186	IO(H)
19	VCCIO(A)	61	IO(C)	103	GND	145	INREF(F)	187	IO(H)
20	IO(A)	62	IO(C)	104	GNDPLL(1)	146	VCC	188	GND
21	GND	63	IO(C)	105	PLLRST(1)	147	IOCTRL(F)	189	VCCIO(H)
22	IO(A)	64	IO(C)	106	VCCPLL(1)	148	IO(F)	190	IO(H)
23	TDI	65	IO(C)	107	IO(E)	149	IO(F)	191	IO(H)
24	CLK(0)	66	IO(C)	108	GND	150	VCCIO(F)	192	IOCTRL(H)
25	CLK(1)	67	IOCTRL(C)	109	IO(E)	151	IO(F)	193	IO(H)
26	VCC	68	INREF(C)	110	IO(E)	152	IO(F)	194	INREF(H)
27	CLK(2)/PLLIN(2)	69	IOCTRL(C)	111	VCCIO(E)	153	GND	195	VCC
28	CLK(3)/PLLIN(1)	70	IO(C)	112	IO(E)	154	IO(F)	196	IOCTRL(H)
29	VCC	71	IO(C)	113	VCC	155	PLLOUT(3)	197	IO(H)
30	CLK(4)/ DEDCLK/PLLIN(0)	72	VCCIO(C)	114	IO(E)	156	GNDPLL(0)	198	IO(H)
31	IO(B)	73	IO(C)	115	IO(E)	157	GND	199	IO(H)
32	IO(B)	74	IO(C)	116	IO(E)	158	VCCPLL(0)	200	IO(H)
33	GND	75	GND	117	IOCTRL(E)	159	PLLRST(0)	201	IO(H)
34	VCCIO(B)	76	VCC	118	INREF(E)	160	GND	202	IO(H)
35	IO(B)	77	IO(C)	119	IOCTRL(E)	161	IO(G)	203	VCCIO(H)
36	IO(B)	78	TRSTB	120	IO(E)	162	VCCIO(G)	204	GND
37	IO(B)	79	VCC	121	IO(E)	163	IO(G)	205	IO(H)
38	IO(B)	80	IO(D)	122	VCCIO(E)	164	IO(G)	206	PLLOUT(2)
39	IOCTRL(B)	81	IO(D)	123	GND	165	VCC	207	GND
40	INREF(B)	82	IO(D)	124	IO(E)	166	IO(G)	208	GNDPLL(3)
41	IOCTRL(B)	83	GND	125	IO(E)	167	IO(G)		
42	IO(B)	84	VCCIO(D)	126	IO(E)	168	IO(G)		

QL6325 - 280 LFBGA Pinout Diagram

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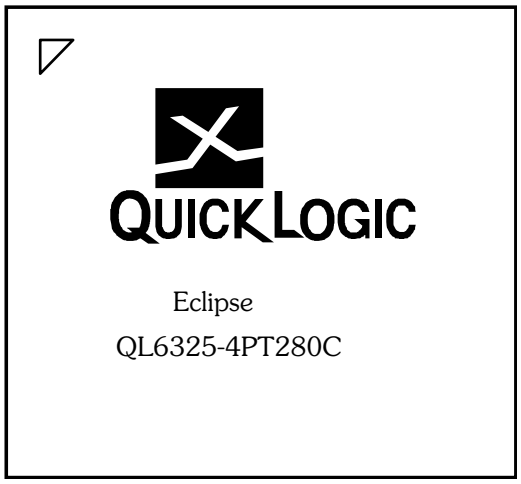

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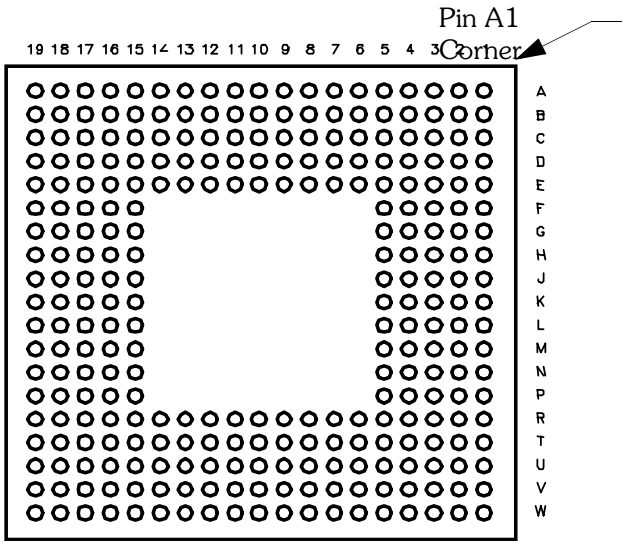

QL6325 - 280 LFBGA Pinout Table

Table 29: 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VCC	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VCC	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VCC	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

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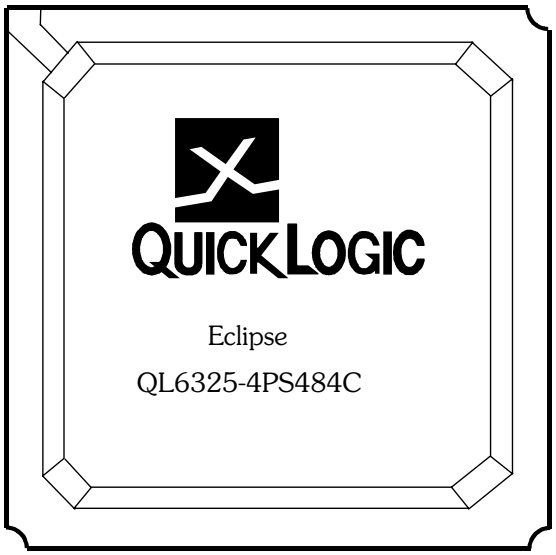

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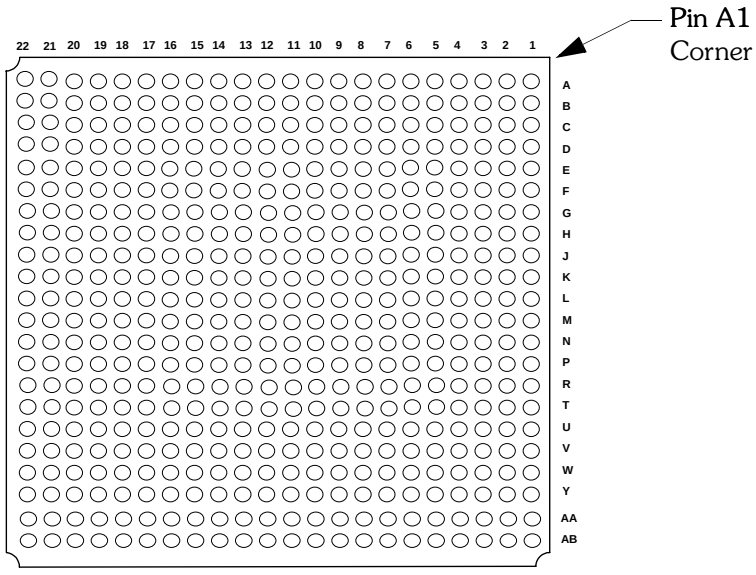

QL6325 - 484 PBGA Pinout Table

Table 30: 484 PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4)/ DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	NC	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	NC	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	VCC	L10	GND
A11	NC	C11	I/O(H)	E11	VDED2	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	VCC	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	I/O(H)	F7	VCCIO(H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	I/O(H)	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	NC	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	NC	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	NC	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	NC	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	NC	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 30: 484 PBGA Pinout Table *(Continued)*

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	I/O(B)	P16	I/O(E)	T9	NC	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	NC	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	NC	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	VCC	R1	I/O(B)	T16	GND	V9	NC	Y2	I/O(B)	AA17	I/O(D)
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	VDED2	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	NC	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLRST(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	NC	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLLRST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	NC	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	NC	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	NC	AA9	I/O(C)		

QL6500 - 280 LFBGA Pinout Diagram

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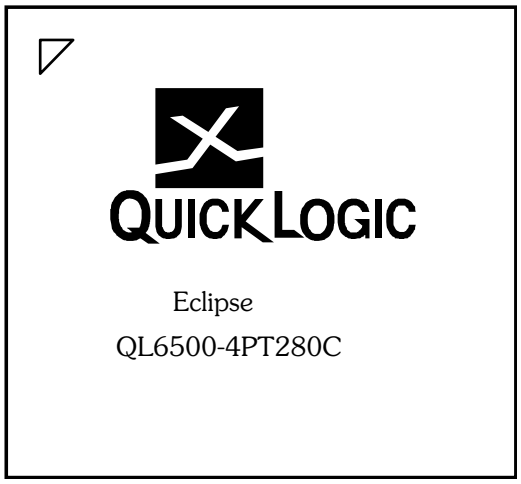

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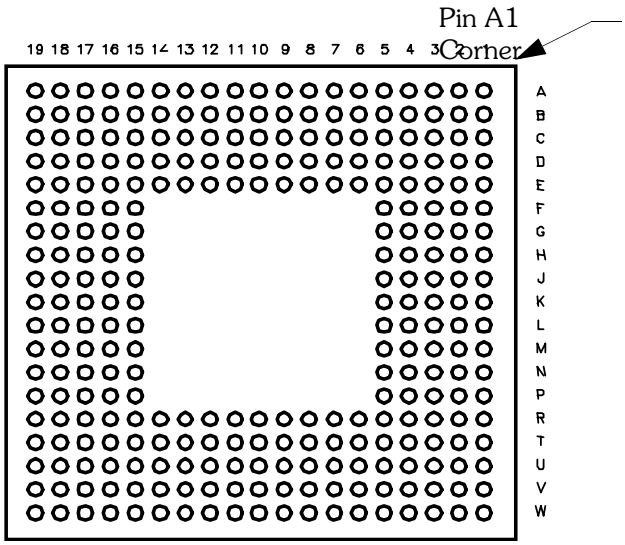

QL6500 - 280 LFBGA Pinout Table

Table 31: 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VCC	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VCC	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VCC	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

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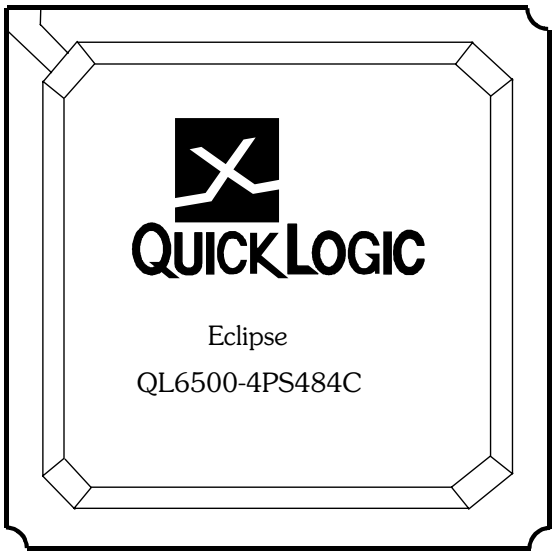

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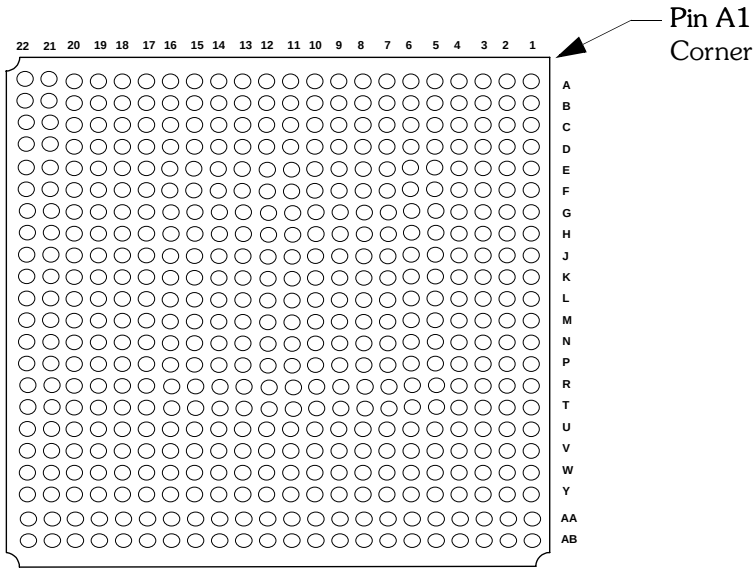


QL6500 - 484 PBGA Pinout Table

Table 32: 484 PBGA Pinout Table

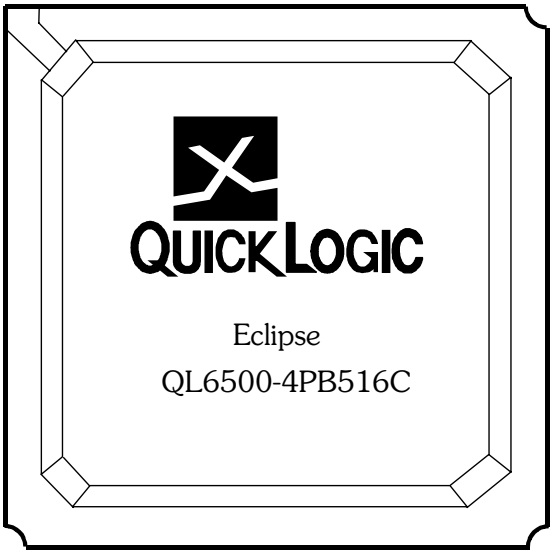
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4)/ DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	I/O(H)	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	I/O(H)	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	VCC	L10	GND
A11	I/O(H)	C11	I/O(H)	E11	VDED2	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	VCC	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	I/O(H)	F7	VCCIO(H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	I/O(H)	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	I/O(G)	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	I/O(G)	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	I/O(G)	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	I/O(G)	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	I/O(G)	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 32: 484 PBGA Pinout Table *(Continued)*

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	I/O(B)	P16	I/O(E)	T9	I/O(C)	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	I/O(C)	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	I/O(D)	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	VCC	R1	I/O(B)	T16	GND	V9	I/O(C)	Y2	I/O(B)	AA17	I/O(D)
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	VDED2	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	I/O(D)	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLRST(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	I/O(C)	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLLRST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	I/O(C)	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	I/O(D)	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	I/O(D)	AA9	I/O(C)		

QL6500 - 516 PBGA Pinout Diagram

Top



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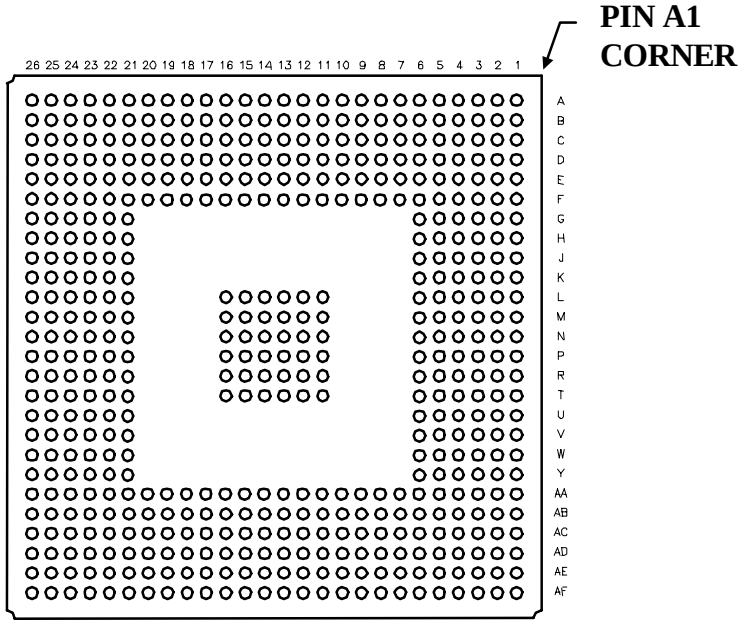

QL6500 - 516 PBGA Pinout Table

Table 33: 516 PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	GND	C1	I/O(F)	E1	I/O(G)	G1	I/O(G)	L5	VCC	P3	I/O(H)
A2	I/O(F)	C2	I/O(F)	E2	I/O(G)	G2	INREF(G)	L6	VCC	P4	VCC
A3	I/O(F)	C3	I/O(F)	E3	I/O(G)	G3	I/O(G)	L11	GND	P5	I/O(H)
A4	I/O(F)	C4	PLLOUT(3)	E4	VCCPLL(0)	G4	I/O(G)	L12	GND	P6	VCCIO(H)
A5	I/O(F)	C5	I/O(F)	E5	I/O(F)	G5	I/O(G)	L13	GND	P11	GND
A6	I/O(F)	C6	I/O(F)	E6	I/O(F)	G6	VCCIO(G)	L14	GND	P12	GND
A7	IOCTRL(F)	C7	I/O(F)	E7	I/O(F)	G21	VCCIO(D)	L15	GND	P13	GND
A8	I/O(F)	C8	INREF(F)	E8	VCC	G22	I/O(D)	L16	GND	P14	GND
A9	I/O(F)	C9	I/O(F)	E9	I/O(F)	G23	I/O(D)	L21	VCC	P15	GND
A10	I/O(F)	C10	I/O(F)	E10	I/O(F)	G24	I/O(D)	L22	I/O(D)	P16	GND
A11	I/O(F)	C11	I/O(F)	E11	I/O(F)	G25	I/O(D)	L23	I/O(D)	P21	VCCIO(C)
A12	I/O(F)	C12	I/O(F)	E12	VCC	G26	INREF(D)	L24	I/O(D)	P22	I/O(C)
A13	I/O(E)	C13	CLK(7)	E13	I/O(F)	H1	I/O(G)	L25	I/O(D)	P23	VCC
A14	I/O(E)	C14	I/O(E)	E14	I/O(F)	H2	I/O(G)	L26	I/O(D)	P24	I/O(C)
A15	I/O(E)	C15	I/O(E)	E15	I/O(E)	H3	IOCTRL(G)	M1	I/O(G)	P25	I/O(C)
A16	I/O(E)	C16	I/O(E)	E16	VCC	H4	I/O(G)	M2	I/O(G)	P26	TRSTB
A17	I/O(E)	C17	I/O(E)	E17	CLK(6)	H5	I/O(G)	M3	I/O(G)	R1	I/O(H)
A18	IOCTRL(E)	C18	I/O(E)	E18	I/O(E)	H6	VCC	M4	I/O(G)	R2	I/O(H)
A19	IOCTRL(E)	C19	I/O(E)	E19	I/O(E)	H21	VCC	M5	I/O(G)	R3	I/O(H)
A20	I/O(E)	C20	I/O(E)	E20	I/O(E)	H22	VCC	M6	VCCIO(G)	R4	I/O(H)
A21	I/O(E)	C21	I/O(E)	E21	I/O(E)	H23	I/O(D)	M11	GND	R5	VCC
A22	I/O(E)	C22	I/O(E)	E22	I/O(E)	H24	IOCTRL(D)	M12	GND	R6	VCC
A23	I/O(E)	C23	I/O(E)	E23	GNDPLL(1)	H25	IOCTRL(D)	M13	GND	R11	GND
A24	I/O(E)	C24	I/O(E)	E24	I/O(E)	H26	I/O(D)	M14	GND	R12	GND
A25	PLLRST(1)	C25	I/O(E)	E25	I/O(D)	J1	I/O(G)	M15	GND	R13	GND
A26	GND	C26	I/O(E)	E26	I/O(D)	J2	I/O(G)	M16	GND	R14	GND
B1	I/O(F)	D1	I/O(G)	F1	IOCTRL(G)	J3	I/O(G)	M21	VCCIO(D)	R15	GND
B2	PLLRST(0)	D2	I/O(G)	F2	I/O(G)	J4	I/O(G)	M22	VCC	R16	GND
B3	I/O(F)	D3	I/O(F)	F3	I/O(G)	J5	I/O(G)	M23	I/O(D)	R21	VCC
B4	I/O(F)	D4	I/O(F)	F4	I/O(G)	J6	VCCIO(G)	M24	I/O(D)	R22	I/O(C)
B5	I/O(F)	D5	GNDPLL(0)	F5	I/O(F)	J21	VCCIO(D)	M25	I/O(D)	R23	I/O(C)
B6	I/O(F)	D6	I/O(F)	F6	GND	J22	I/O(D)	M26	I/O(D)	R24	I/O(C)
B7	IOCTRL(F)	D7	I/O(F)	F7	VCCIO(F)	J23	I/O(D)	N1	TCK	R25	I/O(C)
B8	I/O(F)	D8	I/O(F)	F8	VCC	J24	I/O(D)	N2	I/O(H)	R26	I/O(C)
B9	I/O(F)	D9	I/O(F)	F9	VCCIO(F)	J25	I/O(D)	N3	I/O(G)	T1	I/O(H)
B10	I/O(F)	D10	I/O(F)	F10	GND	J26	I/O(D)	N4	I/O(G)	T2	I/O(H)
B11	I/O(F)	D11	I/O(F)	F11	VCC	K1	I/O(G)	N5	I/O(G)	T3	I/O(H)
B12	I/O(F)	D12	I/O(F)	F12	VCCIO(F)	K2	I/O(G)	N6	GND	T4	I/O(H)
B13	CLK(5)/ PLLIN(3)	D13	TMS	F13	GND	K3	I/O(G)	N11	GND	T5	I/O(H)
B14	I/O(E)	D14	I/O(E)	F14	VCCIO(E)	K4	I/O(G)	N12	GND	T6	VCC
B15	I/O(E)	D15	I/O(E)	F15	VCC	K5	I/O(G)	N13	GND	T11	GND
B16	I/O(E)	D16	I/O(F)	F16	VCC	K6	GND	N14	GND	T12	GND
B17	I/O(E)	D17	I/O(E)	F17	GND	K21	GND	N15	GND	T13	GND
B18	INREF(E)	D18	I/O(F)	F18	VCCIO(E)	K22	I/O(D)	N16	GND	T14	GND
B19	I/O(E)	D19	CLK(8)	F19	VCC	K23	I/O(D)	N21	GND	T15	GND
B20	I/O(E)	D20	I/O(E)	F20	VCCIO(E)	K24	I/O(D)	N22	I/O(D)	T16	GND
B21	I/O(E)	D21	I/O(E)	F21	GND	K25	I/O(D)	N23	I/O(D)	T21	VCC
B22	I/O(E)	D22	I/O(E)	F22	I/O(E)	K26	I/O(D)	N24	I/O(D)	T22	VCC
B23	I/O(E)	D23	VCCPLL(1)	F23	I/O(D)	L1	I/O(G)	N25	I/O(D)	T23	I/O(C)
B24	I/O(E)	D24	I/O(E)	F24	I/O(D)	L2	I/O(G)	N26	I/O(D)	T24	I/O(C)
B25	I/O(E)	D25	I/O(E)	F25	I/O(D)	L3	I/O(G)	P1	I/O(H)	T25	I/O(C)
B26	PLLOUT(0)	D26	I/O(D)	F26	I/O(D)	L4	I/O(G)	P2	I/O(H)	T26	I/O(C)

Table 33: 516 PBGA Pinout Table *(Continued)*

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
U1	I/O(H)	W25	INREF(C)	AA21	GND	AC3	I/O(A)	AD11	I/O(A)	AE19	I/O(B)
U2	I/O(H)	W26	I/O(C)	AA22	VCCPLL(2)	AC4	I/O(A)	AD12	TDI	AE20	I/O(B)
U3	I/O(H)	Y1	I/O(H)	AA23	I/O(C)	AC5	I/O(A)	AD13	CLK(4) DEDCLK/ PLLIN(0)	AE21	I/O(B)
U4	I/O(H)	Y2	I/O(H)	AA24	I/O(C)	AC6	I/O(A)	AD14	I/O(A)	AE22	I/O(B)
U5	I/O(H)	Y3	I/O(H)	AA25	I/O(C)	AC7	I/O(A)	AD15	I/O(B)	AE23	I/O(B)
U6	GND	Y4	I/O(H)	AA26	I/O(C)	AC8	I/O(A)	AD16	I/O(B)	AE24	I/O(B)
U21	GND	Y5	I/O(H)	AB1	I/O(H)	AC9	I/O(A)	AD17	I/O(B)	AE25	PLLRST(2)
U22	I/O(C)	Y6	VCCIO(H)	AB2	I/O(H)	AC10	I/O(A)	AD18	INREF(B)	AE26	I/O(B)
U23	I/O(C)	Y21	VCCIO(C)	AB3	I/O(A)	AC11	I/O(A)	AD19	I/O(B)	AF1	I/O(A)
U24	I/O(C)	Y22	I/O(C)	AB4	GNDPLL(3)	AC12	I/O(A)	AD20	I/O(B)	AF2	I/O(A)
U25	I/O(C)	Y23	I/O(C)	AB5	VCCPLL(3)	AC13	I/O(A)	AD21	I/O(B)	AF3	I/O(A)
U26	I/O(C)	Y24	I/O(C)	AB6	I/O(A)	AC14	CLK(1)	AD22	I/O(B)	AF4	I/O(A)
V1	I/O(H)	Y25	I/O(C)	AB7	I/O(A)	AC15	I/O(B)	AD23	I/O(B)	AF5	I/O(A)
V2	IOCTRL(H)	Y26	IOCTRL(C)	AB8	I/O(A)	AC16	I/O(B)	AD24	GND	AF6	IOCTRL(A)
V3	IOCTRL(H)	AA1	I/O(H)	AB9	I/O(A)	AC17	I/O(B)	AD25	I/O(B)	AF7	I/O(A)
V4	I/O(H)	AA2	I/O(H)	AB10	I/O(A)	AC18	I/O(B)	AD26	I/O(B)	AF8	I/O(A)
V5	I/O(H)	AA3	I/O(H)	AB11	VCC	AC19	I/O(B)	AE1	GND	AF9	I/O(A)
V6	VCCIO(H)	AA4	I/O(A)	AB12	I/O(A)	AC20	I/O(B)	AE2	GND	AF10	I/O(A)
V21	VCCIO(C)	AA5	I/O(A)	AB13	I/O(A)	AC21	I/O(B)	AE3	I/O(A)	AF11	I/O(A)
V22	I/O(C)	AA6	GND	AB14	CLK(3)/ PLLIN(1)	AC22	TDO	AE4	I/O(A)	AF12	CLK(2)/ PLLIN(2)
V23	I/O(C)	AA7	VCCIO(A)	AB15	VCC	AC23	PLLOUT(1)	AE5	I/O(A)	AF13	I/O(B)
V24	IOCTRL(C)	AA8	VCC	AB16	I/O(B)	AC24	I/O(B)	AE6	I/O(A)	AF14	I/O(B)
V25	I/O(C)	AA9	VCCIO(A)	AB17	I/O(B)	AC25	I/O(B)	AE7	INREF(A)	AF15	I/O(B)
V26	I/O(C)	AA10	GND	AB18	I/O(B)	AC26	I/O(C)	AE8	I/O(A)	AF16	I/O(B)
W1	INREF(H)	AA11	VCC	AB19	VCC	AD1	I/O(A)	AE9	I/O(A)	AF17	I/O(B)
W2	I/O(H)	AA12	VCCIO(A)	AB20	I/O(B)	AD2	PLLOUT(2)	AE10	I/O(A)	AF18	I/O(B)
W3	I/O(H)	AA13	GND	AB21	I/O(B)	AD3	PLLRST(3)	AE11	I/O(A)	AF19	IOCTRL(B)
W4	I/O(H)	AA14	VCCIO(B)	AB22	GNDPLL(2)	AD4	I/O(A)	AE12	CLK(0)	AF20	IOCTRL(B)
W5	VCC	AA15	VCC	AB23	I/O(B)	AD5	I/O(A)	AE13	I/O(B)	AF21	I/O(B)
W6	VCC	AA16	VCC	AB24	I/O(C)	AD6	I/O(A)	AE14	I/O(B)	AF22	I/O(B)
W21	VCC	AA17	GND	AB25	I/O(C)	AD7	I/O(A)	AE15	I/O(B)	AF23	I/O(B)
W22	I/O(C)	AA18	VCCIO(B)	AB26	I/O(C)	AD8	IOCTRL(A)	AE16	I/O(B)	AF24	I/O(B)
W23	I/O(C)	AA19	VCC	AC1	I/O(A)	AD9	I/O(A)	AE17	I/O(B)	AF25	I/O(B)
W24	I/O(C)	AA20	VCCIO(B)	AC2	I/O(A)	AD10	I/O(A)	AE18	I/O(B)	AF26	I/O(B)

QL6600 - 280 LFBGA Pinout Diagram

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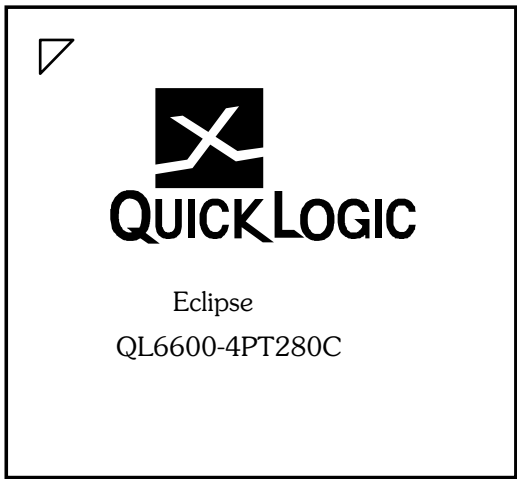

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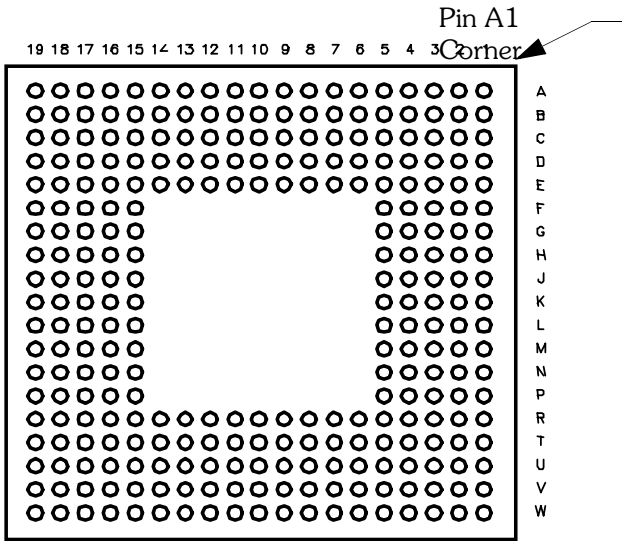

QL6600 - 280 LFBGA Pinout Table

Table 34: 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VCC	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VCC	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VCC	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

QL6600 - 484 PBGA Pinout Diagram

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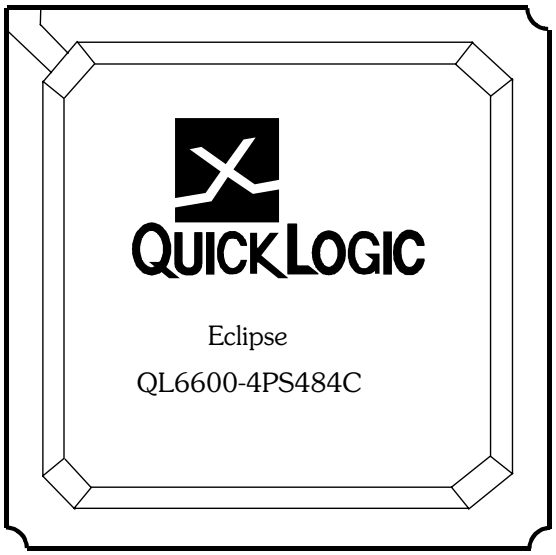

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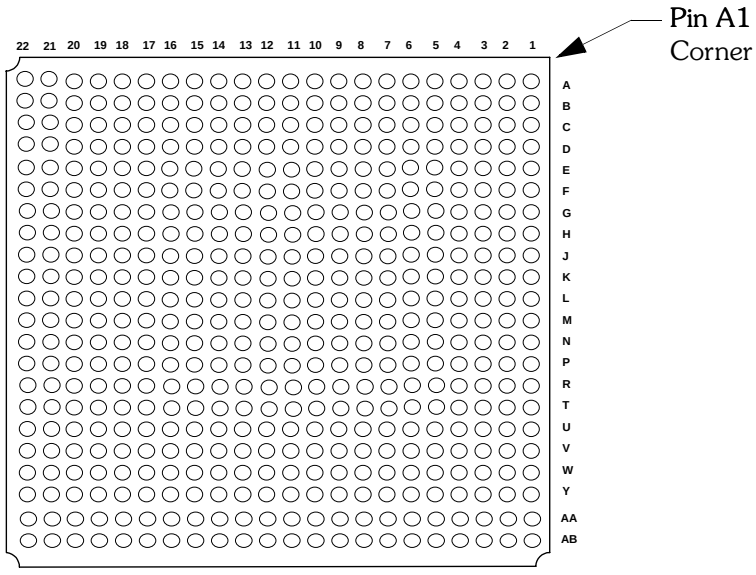


QL6600 - 484 PBGA Pinout Table

Table 35: 484 PBGA Pinout Table

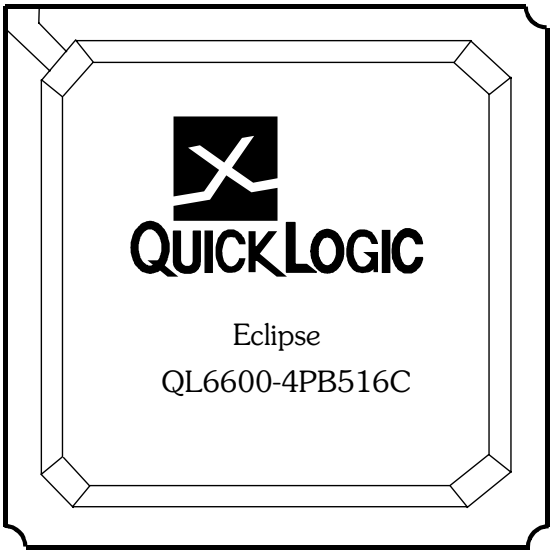
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4)/ DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	I/O(H)	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	I/O(H)	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	VCC	L10	GND
A11	I/O(H)	C11	I/O(H)	E11	VDED2	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	VCC	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	I/O(H)	F7	VCCIO(H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	I/O(H)	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	I/O(G)	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	I/O(G)	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	I/O(G)	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	I/O(G)	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	I/O(G)	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 35: 484 PBGA Pinout Table *(Continued)*

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	I/O(B)	P16	I/O(E)	T9	I/O(C)	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	I/O(C)	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	I/O(D)	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	VCC	R1	I/O(B)	T16	GND	V9	I/O(C)	Y2	I/O(B)	AA17	I/O(D)
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	VDED2	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	I/O(D)	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLRST(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	I/O(C)	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLLRST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	I/O(C)	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	I/O(D)	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	I/O(D)	AA9	I/O(C)		

QL6600 - 516 PBGA Pinout Diagram

Top



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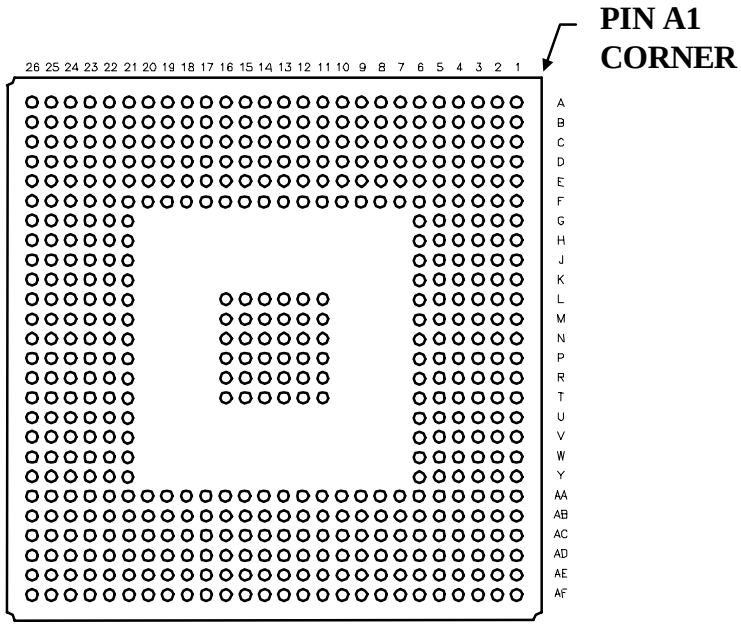


QL6600 - 516 PBGA Pinout Table

Table 36: 516 PBGA Pinout Table

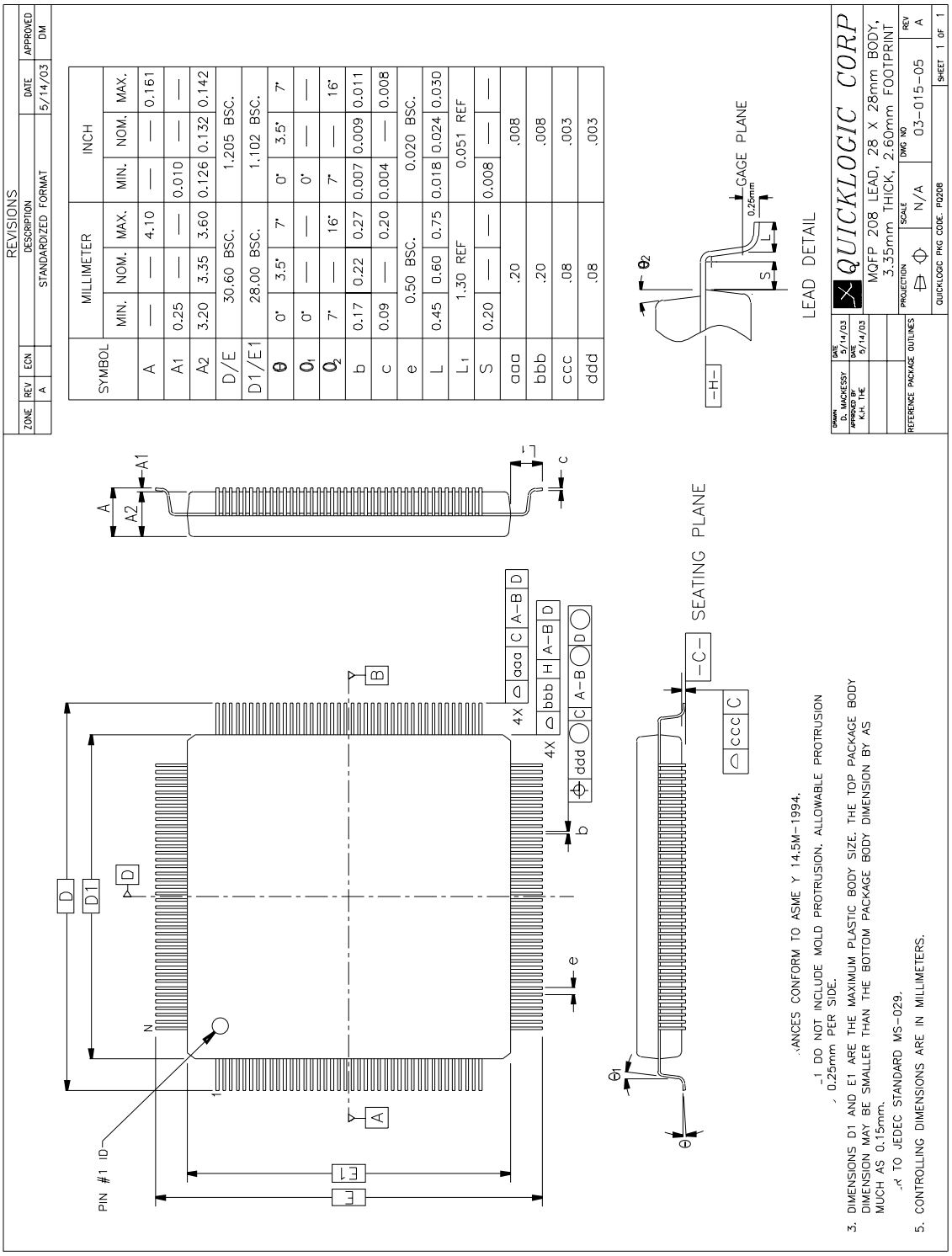
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	GND	C1	I/O(F)	E1	I/O(G)	G1	I/O(G)	L5	VCC	P3	I/O(H)
A2	I/O(F)	C2	I/O(F)	E2	I/O(G)	G2	INREF(G)	L6	VCC	P4	VCC
A3	I/O(F)	C3	I/O(F)	E3	I/O(G)	G3	I/O(G)	L11	GND	P5	I/O(H)
A4	I/O(F)	C4	PLLOUT(3)	E4	VCCPLL(0)	G4	I/O(G)	L12	GND	P6	VCCIO(H)
A5	I/O(F)	C5	I/O(F)	E5	I/O(F)	G5	I/O(G)	L13	GND	P11	GND
A6	I/O(F)	C6	I/O(F)	E6	I/O(F)	G6	VCCIO(G)	L14	GND	P12	GND
A7	IOCTRL(F)	C7	I/O(F)	E7	I/O(F)	G21	VCCIO(D)	L15	GND	P13	GND
A8	I/O(F)	C8	INREF(F)	E8	VCC	G22	I/O(D)	L16	GND	P14	GND
A9	I/O(F)	C9	I/O(F)	E9	I/O(F)	G23	I/O(D)	L21	VCC	P15	GND
A10	I/O(F)	C10	I/O(F)	E10	I/O(F)	G24	I/O(D)	L22	I/O(D)	P16	GND
A11	I/O(F)	C11	I/O(F)	E11	I/O(F)	G25	I/O(D)	L23	I/O(D)	P21	VCCIO(C)
A12	I/O(F)	C12	I/O(F)	E12	VCC	G26	INREF(D)	L24	I/O(D)	P22	I/O(C)
A13	I/O(E)	C13	CLK(7)	E13	I/O(F)	H1	I/O(G)	L25	I/O(D)	P23	VCC
A14	I/O(E)	C14	I/O(E)	E14	I/O(F)	H2	I/O(G)	L26	I/O(D)	P24	I/O(C)
A15	I/O(E)	C15	I/O(E)	E15	I/O(E)	H3	IOCTRL(G)	M1	I/O(G)	P25	I/O(C)
A16	I/O(E)	C16	I/O(E)	E16	VCC	H4	I/O(G)	M2	I/O(G)	P26	TRSTB
A17	I/O(E)	C17	I/O(E)	E17	CLK(6)	H5	I/O(G)	M3	I/O(G)	R1	I/O(H)
A18	IOCTRL(E)	C18	I/O(E)	E18	I/O(E)	H6	VCC	M4	I/O(G)	R2	I/O(H)
A19	IOCTRL(E)	C19	I/O(E)	E19	I/O(E)	H21	VCC	M5	I/O(G)	R3	I/O(H)
A20	I/O(E)	C20	I/O(E)	E20	I/O(E)	H22	VCC	M6	VCCIO(G)	R4	I/O(H)
A21	I/O(E)	C21	I/O(E)	E21	I/O(E)	H23	I/O(D)	M11	GND	R5	VCC
A22	I/O(E)	C22	I/O(E)	E22	I/O(E)	H24	IOCTRL(D)	M12	GND	R6	VCC
A23	I/O(E)	C23	I/O(E)	E23	GNDPLL(1)	H25	IOCTRL(D)	M13	GND	R11	GND
A24	I/O(E)	C24	I/O(E)	E24	I/O(E)	H26	I/O(D)	M14	GND	R12	GND
A25	PLLRST(1)	C25	I/O(E)	E25	I/O(D)	J1	I/O(G)	M15	GND	R13	GND
A26	GND	C26	I/O(E)	E26	I/O(D)	J2	I/O(G)	M16	GND	R14	GND
B1	I/O(F)	D1	I/O(G)	F1	IOCTRL(G)	J3	I/O(G)	M21	VCCIO(D)	R15	GND
B2	PLLRST(0)	D2	I/O(G)	F2	I/O(G)	J4	I/O(G)	M22	VCC	R16	GND
B3	I/O(F)	D3	I/O(F)	F3	I/O(G)	J5	I/O(G)	M23	I/O(D)	R21	VCC
B4	I/O(F)	D4	I/O(F)	F4	I/O(G)	J6	VCCIO(G)	M24	I/O(D)	R22	I/O(C)
B5	I/O(F)	D5	GNDPLL(0)	F5	I/O(F)	J21	VCCIO(D)	M25	I/O(D)	R23	I/O(C)
B6	I/O(F)	D6	I/O(F)	F6	GND	J22	I/O(D)	M26	I/O(D)	R24	I/O(C)
B7	IOCTRL(F)	D7	I/O(F)	F7	VCCIO(F)	J23	I/O(D)	N1	TCK	R25	I/O(C)
B8	I/O(F)	D8	I/O(F)	F8	VCC	J24	I/O(D)	N2	I/O(H)	R26	I/O(C)
B9	I/O(F)	D9	I/O(F)	F9	VCCIO(F)	J25	I/O(D)	N3	I/O(G)	T1	I/O(H)
B10	I/O(F)	D10	I/O(F)	F10	GND	J26	I/O(D)	N4	I/O(G)	T2	I/O(H)
B11	I/O(F)	D11	I/O(F)	F11	VCC	K1	I/O(G)	N5	I/O(G)	T3	I/O(H)
B12	I/O(F)	D12	I/O(F)	F12	VCCIO(F)	K2	I/O(G)	N6	GND	T4	I/O(H)
B13	CLK(5)/ PLLIN(3)	D13	TMS	F13	GND	K3	I/O(G)	N11	GND	T5	I/O(H)
B14	I/O(E)	D14	I/O(E)	F14	VCCIO(E)	K4	I/O(G)	N12	GND	T6	VCC
B15	I/O(E)	D15	I/O(E)	F15	VCC	K5	I/O(G)	N13	GND	T11	GND
B16	I/O(E)	D16	I/O(F)	F16	VCC	K6	GND	N14	GND	T12	GND
B17	I/O(E)	D17	I/O(E)	F17	GND	K21	GND	N15	GND	T13	GND
B18	INREF(E)	D18	I/O(F)	F18	VCCIO(E)	K22	I/O(D)	N16	GND	T14	GND
B19	I/O(E)	D19	CLK(8)	F19	VCC	K23	I/O(D)	N21	GND	T15	GND
B20	I/O(E)	D20	I/O(E)	F20	VCCIO(E)	K24	I/O(D)	N22	I/O(D)	T16	GND
B21	I/O(E)	D21	I/O(E)	F21	GND	K25	I/O(D)	N23	I/O(D)	T21	VCC
B22	I/O(E)	D22	I/O(E)	F22	I/O(E)	K26	I/O(D)	N24	I/O(D)	T22	VCC
B23	I/O(E)	D23	VCCPLL(1)	F23	I/O(D)	L1	I/O(G)	N25	I/O(D)	T23	I/O(C)
B24	I/O(E)	D24	I/O(E)	F24	I/O(D)	L2	I/O(G)	N26	I/O(D)	T24	I/O(C)
B25	I/O(E)	D25	I/O(E)	F25	I/O(D)	L3	I/O(G)	P1	I/O(H)	T25	I/O(C)
B26	PLLOUT(0)	D26	I/O(D)	F26	I/O(D)	L4	I/O(G)	P2	I/O(H)	T26	I/O(C)

Table 36: 516 PBGA Pinout Table *(Continued)*

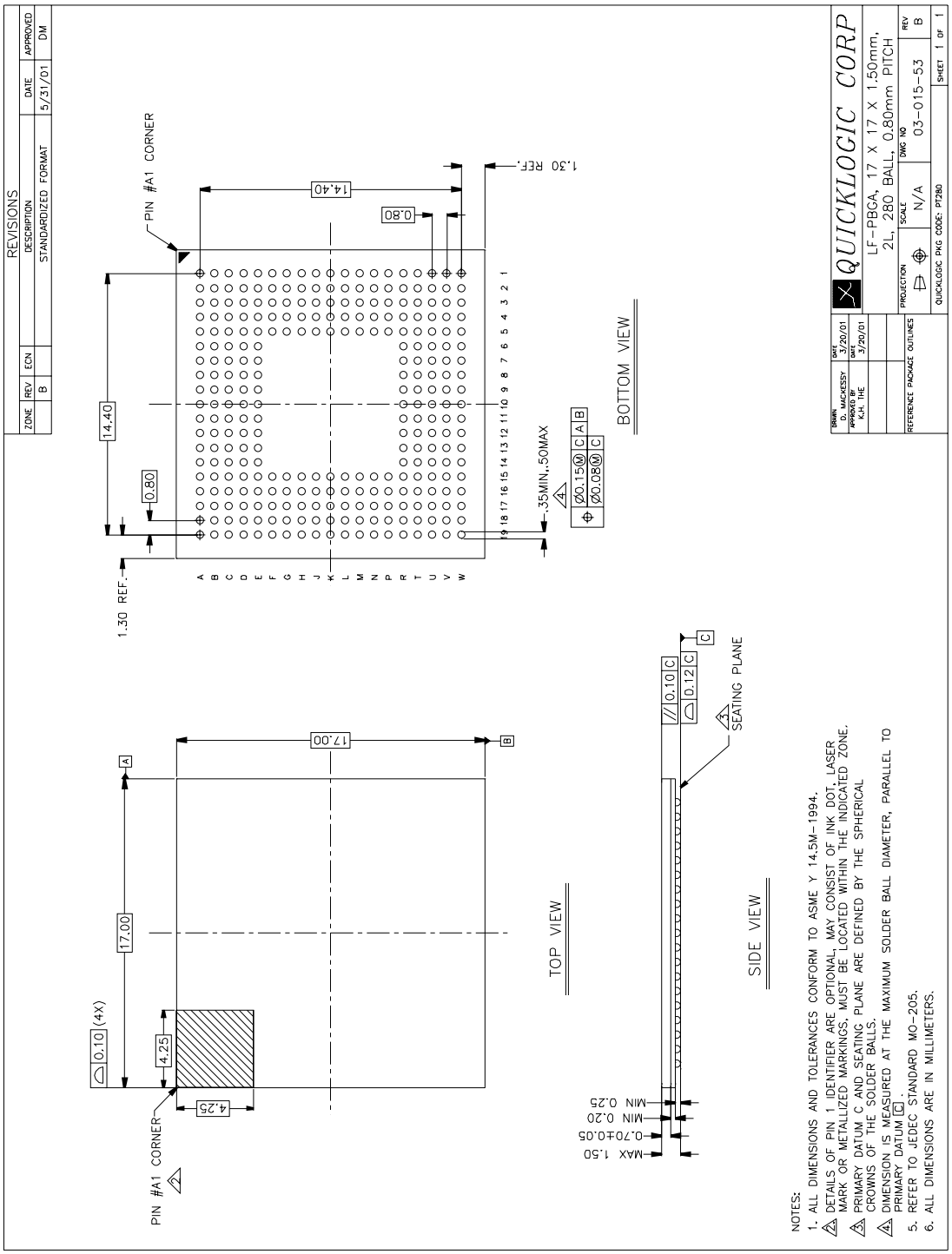
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
U1	I/O(H)	W25	INREF(C)	AA21	GND	AC3	I/O(A)	AD11	I/O(A)	AE19	I/O(B)
U2	I/O(H)	W26	I/O(C)	AA22	VCCPLL(2)	AC4	I/O(A)	AD12	TDI	AE20	I/O(B)
U3	I/O(H)	Y1	I/O(H)	AA23	I/O(C)	AC5	I/O(A)	AD13	CLK(4) DEDCLK/ PLLIN(0)	AE21	I/O(B)
U4	I/O(H)	Y2	I/O(H)	AA24	I/O(C)	AC6	I/O(A)	AD14	I/O(A)	AE22	I/O(B)
U5	I/O(H)	Y3	I/O(H)	AA25	I/O(C)	AC7	I/O(A)	AD15	I/O(B)	AE23	I/O(B)
U6	GND	Y4	I/O(H)	AA26	I/O(C)	AC8	I/O(A)	AD16	I/O(B)	AE24	I/O(B)
U21	GND	Y5	I/O(H)	AB1	I/O(H)	AC9	I/O(A)	AD17	I/O(B)	AE25	PLLRST(2)
U22	I/O(C)	Y6	VCCIO(H)	AB2	I/O(H)	AC10	I/O(A)	AD18	INREF(B)	AE26	I/O(B)
U23	I/O(C)	Y21	VCCIO(C)	AB3	I/O(A)	AC11	I/O(A)	AD19	I/O(B)	AF1	I/O(A)
U24	I/O(C)	Y22	I/O(C)	AB4	GNDPLL(3)	AC12	I/O(A)	AD20	I/O(B)	AF2	I/O(A)
U25	I/O(C)	Y23	I/O(C)	AB5	VCCPLL(3)	AC13	I/O(A)	AD21	I/O(B)	AF3	I/O(A)
U26	I/O(C)	Y24	I/O(C)	AB6	I/O(A)	AC14	CLK(1)	AD22	I/O(B)	AF4	I/O(A)
V1	I/O(H)	Y25	I/O(C)	AB7	I/O(A)	AC15	I/O(B)	AD23	I/O(B)	AF5	I/O(A)
V2	IOCTRL(H)	Y26	IOCTRL(C)	AB8	I/O(A)	AC16	I/O(B)	AD24	GND	AF6	IOCTRL(A)
V3	IOCTRL(H)	AA1	I/O(H)	AB9	I/O(A)	AC17	I/O(B)	AD25	I/O(B)	AF7	I/O(A)
V4	I/O(H)	AA2	I/O(H)	AB10	I/O(A)	AC18	I/O(B)	AD26	I/O(B)	AF8	I/O(A)
V5	I/O(H)	AA3	I/O(H)	AB11	VCC	AC19	I/O(B)	AE1	GND	AF9	I/O(A)
V6	VCCIO(H)	AA4	I/O(A)	AB12	I/O(A)	AC20	I/O(B)	AE2	GND	AF10	I/O(A)
V21	VCCIO(C)	AA5	I/O(A)	AB13	I/O(A)	AC21	I/O(B)	AE3	I/O(A)	AF11	I/O(A)
V22	I/O(C)	AA6	GND	AB14	CLK(3)/ PLLIN(1)	AC22	TDO	AE4	I/O(A)	AF12	CLK(2)/ PLLIN(2)
V23	I/O(C)	AA7	VCCIO(A)	AB15	VCC	AC23	PLLOUT(1)	AE5	I/O(A)	AF13	I/O(B)
V24	IOCTRL(C)	AA8	VCC	AB16	I/O(B)	AC24	I/O(B)	AE6	I/O(A)	AF14	I/O(B)
V25	I/O(C)	AA9	VCCIO(A)	AB17	I/O(B)	AC25	I/O(B)	AE7	INREF(A)	AF15	I/O(B)
V26	I/O(C)	AA10	GND	AB18	I/O(B)	AC26	I/O(C)	AE8	I/O(A)	AF16	I/O(B)
W1	INREF(H)	AA11	VCC	AB19	VCC	AD1	I/O(A)	AE9	I/O(A)	AF17	I/O(B)
W2	I/O(H)	AA12	VCCIO(A)	AB20	I/O(B)	AD2	PLLOUT(2)	AE10	I/O(A)	AF18	I/O(B)
W3	I/O(H)	AA13	GND	AB21	I/O(B)	AD3	PLLRST(3)	AE11	I/O(A)	AF19	IOCTRL(B)
W4	I/O(H)	AA14	VCCIO(B)	AB22	GNDPLL(2)	AD4	I/O(A)	AE12	CLK(0)	AF20	IOCTRL(B)
W5	VCC	AA15	VCC	AB23	I/O(B)	AD5	I/O(A)	AE13	I/O(B)	AF21	I/O(B)
W6	VCC	AA16	VCC	AB24	I/O(C)	AD6	I/O(A)	AE14	I/O(B)	AF22	I/O(B)
W21	VCC	AA17	GND	AB25	I/O(C)	AD7	I/O(A)	AE15	I/O(B)	AF23	I/O(B)
W22	I/O(C)	AA18	VCCIO(B)	AB26	I/O(C)	AD8	IOCTRL(A)	AE16	I/O(B)	AF24	I/O(B)
W23	I/O(C)	AA19	VCC	AC1	I/O(A)	AD9	I/O(A)	AE17	I/O(B)	AF25	I/O(B)
W24	I/O(C)	AA20	VCCIO(B)	AC2	I/O(A)	AD10	I/O(A)	AE18	I/O(B)	AF26	I/O(B)

Package Mechanical Drawings

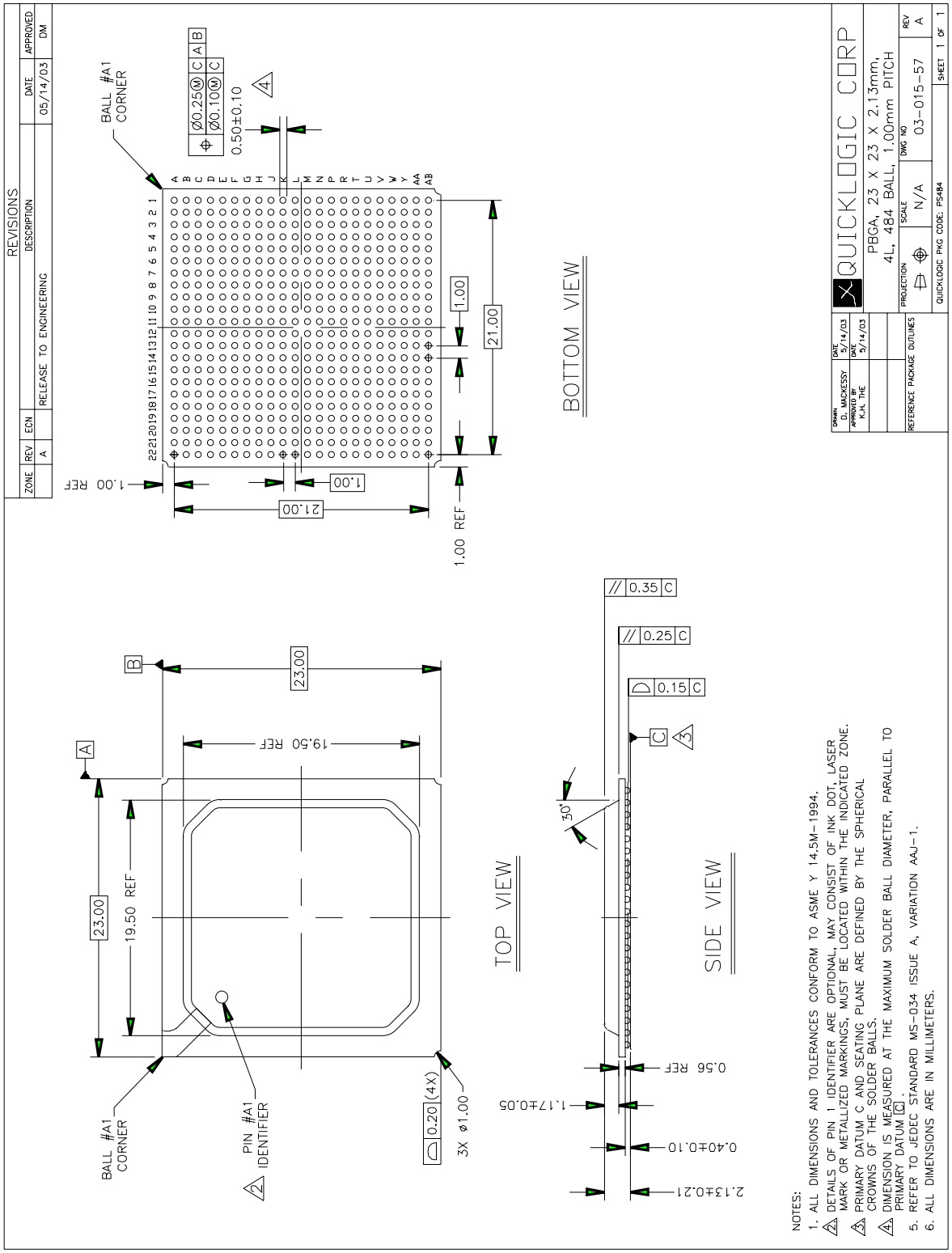
208 PQFP Packaging Drawing



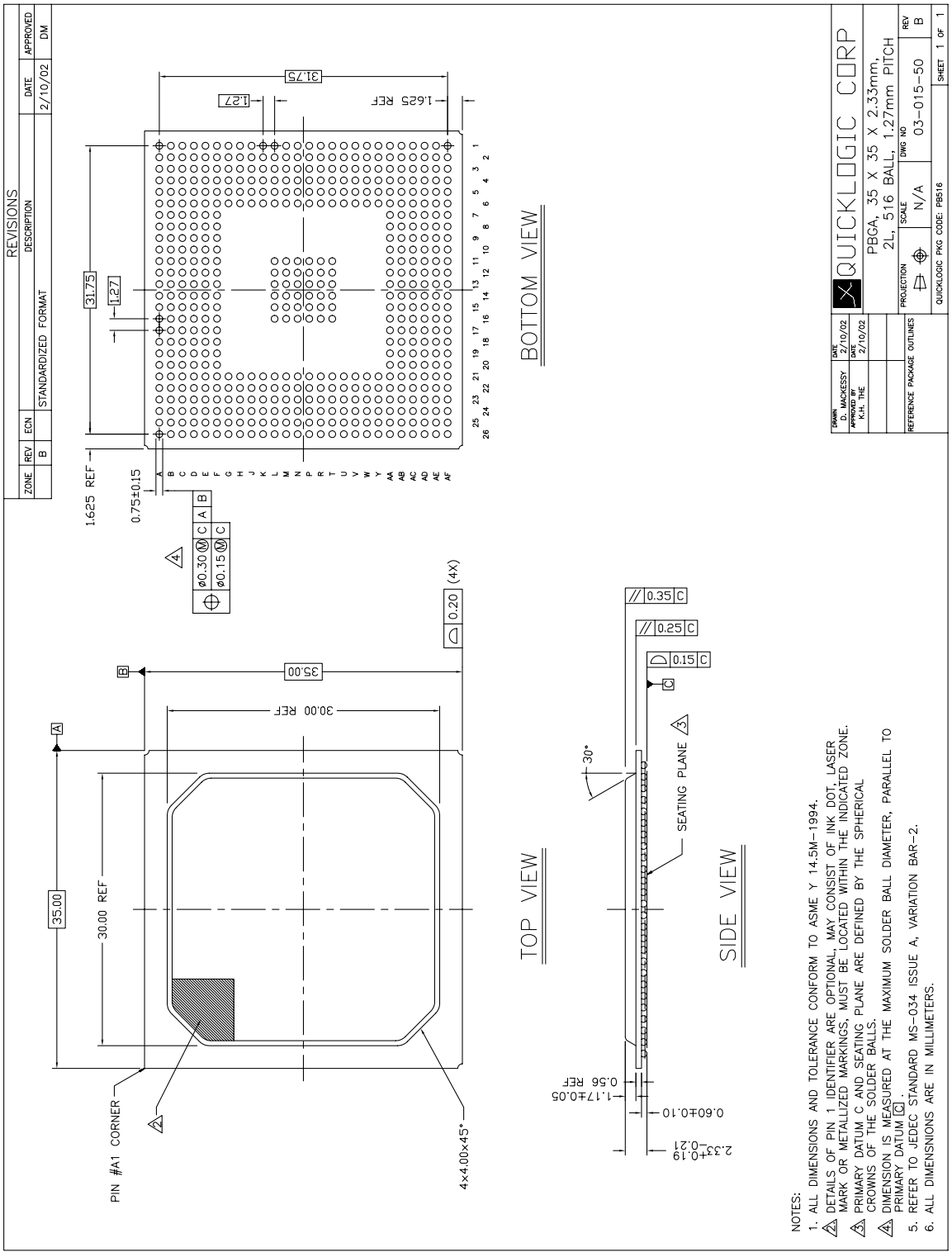
280 LFBGA Packaging Drawing



484 PBGA Packaging Drawing



516 PBGA Packaging Drawing



Packaging Information

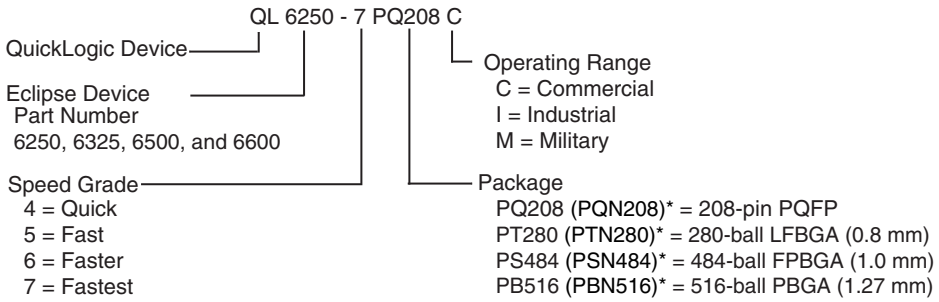
Eclipse product is offered in the following packages. All packages support commercial, industrial, and military temperature ranges. The Eclipse product family packaging information is presented in **Table 37**.

Table 37: Packaging Options

Device Information	QL6250 and QL6325		QL6500 and QL6600	
	Pin/Ball	Pitch	Pin/Ball	Pitch
Package Definitions[a]	208 PQFP	0.50 mm	280 LFBGA	0.80 mm
	280 LFBGA	0.80 mm	484 PBGA	1.0 mm
	484 PBGA	1.0 mm	516 PBGA	1.27 mm

a. PQFP = Plastic Quad Flat Pack
LFBGA = Low Profile Fine Pitch Ball Grid Array
PBGA = Plastic Ball Grid Array

Ordering Information



* Lead-free packaging is available, contact QuickLogic regarding availability (see Contact Information).

Contact Information

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Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Comments
A	Jan 2002	First release.
B	April 2003	Brian Faith and Kathleen Murchek
C	May 2003	Brian Faith and Kathleen Murchek
D	September 2005	Brian Faith, Mehul Kochar, and Kathleen Murchek Combined previous Eclipse Family data sheet with QL6250, QL6325, QL6500, and QL6600 data sheets to create one complete Eclipse Family Data Sheet.
E	March 2007	Jason Lew and Kathleen Murchek Changed pin G16 from VPUMP to GND in all PS484 pinout tables.
F	September 2007	Kathleen Murchek Updated packaging information to include lead-free parts. Updated banner and logo.

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